1 Introduction

The aXiom AX112A-2D is an Automotive Qualified Capacitive Multi-touch controller with the very highest performance, for use in demanding applications across markets such as Automotive, Industrial, White Goods and Medical.

The high performance acquisition engine enables the touchscreen controller to sense regular contacts and gloves. It also allows designers to use thick plastic front lenses and even to sense through a small air gap. Industry leading water rejection and wet finger tracking is also included.

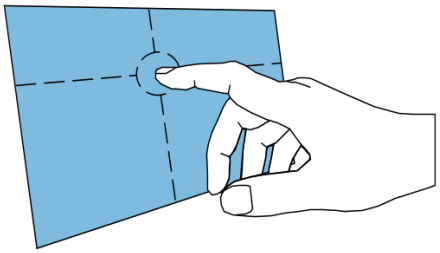

Figure 1-1: aXiom 2D Touch Sensing

A Windows™ based software package, TouchHub2, is provided with the AX112A-2D to ease design and tuning tasks. This allows the designer to input simplified design choices and enables TouchHub2 to automatically create optimized tuning configurations. Additionally, a digitizer driver is available for Linux.

Features at a Glance

Capacitive Multi-touch Controller

- Ultra high SNR: >80dB.
- Supports up to 112 touch sensing channels.
- Flexible channel routing allows arbitrary touch sensor aspect ratios.
- Supports non-rectangular sensors.
- Touch sensing through very thick plastic lenses and/or air gaps.
- Supports non-uniform lens thickness.
- All touches reported at a frame rate of up to 250Hz[1].
- Glove support without switching modes.
- Water suppression and wet finger tracking.
- Low emissions, low drive amplitude, high immunity to conducted interference.
- Host connection using SPI or I^2C slave with interrupt.
- 3V3 and 1V8 supply, no high voltage generators needed.
- Independent I/O voltage supporting 1.8V to 3.3V host signaling.
- Optional external synchronization with display drivers for highest SNR.

General

- Register based tuning with non-volatile configuration storage.
- Field upgradable firmware.
- Sophisticated Built-In-Self-Test routines and diagnostics.
- Automotive AEC-Q100 grade 2 qualified.
- -40°C to +105°C ambient operating temperature.
- Available in LQFP156 package.
- TouchHub2 evaluation and support software for design and tuning.

[1] Subject to configuration.

2 Ordering Information

Device	Package	Part Number	Shipping
AX112A-2D LQFP156 Industrial	LQFP156 Exposed Pad 14x20x1.4mm 0.4 Pitch	838-010011	72 devices per tray
AX112A-2D LQFP156 Automotive	LQFP156 Exposed Pad 14x20x1.4mm 0.4 Pitch	838-010010	72 devices per tray

NOTE: These devices will arrive with default bootloader and firmware installed, you will then need to load your chosen firmware version once mounted on your PCB.

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3.1 Pin Map

3.1.1 LQFP156

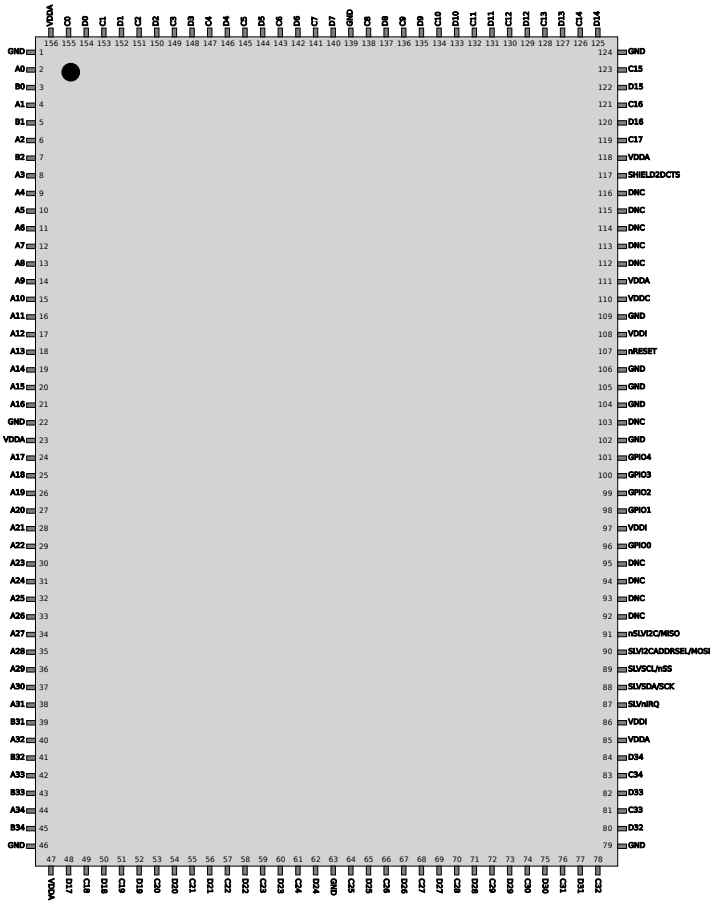

Figure 3.1.1-1: LQFP156 Device Pinout (top view)

3.2 Pin Table

3.2.1 LQFP156

Pin Number	Name	Class	Domain	Function	If not required	Notes
1	GND	PWR		Supply and signal reference	Not applicable	
2	A0	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
3	B0	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
4	A1	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
5	B1	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
6	A2	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
7	B2	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
8	A3	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
9	A4	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
10	A5	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
11	A6	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
12	A7	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
13	A8	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
14	A9	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
15	A10	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
16	A11	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
17	A12	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
18	A13	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
19	A14	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
20	A15	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
21	A16	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
22	GND	PWR		Supply and signal reference	Not applicable	
23	VDDA	PWR		Analogue supply	Not applicable	
24	A17	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
25	A18	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
26	A19	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
27	A20	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
28	A21	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
29	A22	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
30	A23	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
31	A24	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
32	A25	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
33	A26	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
34	A27	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
35	A28	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
36	A29	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
37	A30	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
38	A31	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
39	B31	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
40	A32	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
41	B32	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
42	A33	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
43	B33	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
44	A34	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
45	B34	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
46	GND	PWR		Supply and signal reference	Not applicable	
47	VDDA	PWR		Analogue supply	Not applicable	
48	D17	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
49	C18	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
50	D18	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
51	C19	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
52	D19	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
53	C20	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
54	D20	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
55	C21	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
56	D21	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
57	C22	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
58	D22	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
59	C23	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
60	D23	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
61	C24	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
62	D24	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
63	GND	PWR		Supply and signal reference	Not applicable	
64	C25	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
65	D25	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	

Pin Number	Name	Class	Domain	Function	If not required	Notes
66	C26	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
67	D26	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
68	C27	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
69	D27	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
70	C28	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
71	D28	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
72	C29	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
73	D29	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
74	C30	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
75	D30	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
76	C31	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
77	D31	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
78	C32	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
79	GND	PWR		Supply and signal reference	Not applicable	
80	D32	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
81	C33	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
82	D33	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
83	C34	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
84	D34	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
85	VDDA	PWR		Analogue supply	Not applicable	
86	VDDI	PWR		I/O supply	Not applicable	
87	SLVnIRQ	OD	VDDI	Slave report ready interrupt	Leave no connect	Requires additional pull up if used.
88	SLVSDA / SCK	ODwpu (may change to Iwpu during startup)	VDDI	Slave I^2C data OR SPI SCK	Not applicable	Requires additional pull up if using I^2C mode.
89	SLVSCL / nSS	ODwpu (may change to Iwpu during startup)	VDDI	Slave I^2C clock OR SPI nSS	Not applicable	Requires additional pull up if using I^2C mode.
90	SLVI2CADDRSEL / MOSI	Iwpu	VDDI	Slave I^2C address select OR SPI MOSI	Not applicable	In I^2C mode, controls address. In SPI mode becomes MOSI input from host.
91	nSLVI2C / MISO	Iwpu (may change to O during startup)	VDDI	Slave I^2C mode OR SPI MISO	Not applicable	Sampled at reset; if low selects I^2C mode, if high selects SPI mode and becomes MISO output to host.
92	DNC			Do not connect		
93	DNC			Do not connect		
94	DNC			Do not connect		
95	DNC			Do not connect		
96	GPIO0	IOwpu	VDDI	General purpose I/O	Leave no connect	
97	VDDI	PWR		I/O supply	Not applicable	
98	GPIO1	IOwpu	VDDI	General purpose I/O	Leave no connect	Optionally serves as HSYNC input.
99	GPIO2	IOwpu	VDDI	General purpose I/O	Leave no connect	Optionally serves as VSYNC/EXTSYNC input.
100	GPIO3	IOwpu	VDDI	General purpose I/O	Leave no connect	
101	GPIO4	IOwpu	VDDI	General purpose I/O	Leave no connect	
102	GND	PWR		Supply and signal reference	Not applicable	
103	DNC			Do not connect		
104	GND	PWR		Supply and signal reference	Not applicable	
105	GND	PWR		Supply and signal reference	Not applicable	
106	GND	PWR		Supply and signal reference	Not applicable	
107	nRESET	Iwpu	VDDI	Hardware reset	Not applicable	May require additional bypass capacitor to GND for best EMC.
108	VDDI	PWR		I/O supply	Not applicable	
109	GND	PWR		Supply and signal reference	Not applicable	
110	VDDC	PWR		Core supply		Output from internal LDO.
111	VDDA	PWR		Analogue supply	Not applicable	
112	DNC			Do not connect		
113	DNC			Do not connect		
114	DNC			Do not connect		
115	DNC			Do not connect		
116	DNC			Do not connect		
117	SHIELD2DCTS	AO	VDDA	2DCTS shield pin	Not applicable	Shield driver for 2DCTS sense pins.
118	VDDA	PWR		Analogue supply	Not applicable	
119	C17	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
120	D16	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
121	C16	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
122	D15	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
123	C15	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
124	GND	PWR		Supply and signal reference	Not applicable	
125	D14	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
126	C14	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
127	D13	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
128	C13	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
129	D12	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
130	C12	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	

Pin Number	Name	Class	Domain	Function	If not required	Notes
131	D11	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
132	C11	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
133	D10	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
134	C10	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
135	D9	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
136	C9	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
137	D8	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
138	C8	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
139	GND	PWR		Supply and signal reference	Not applicable	
140	D7	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
141	C7	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
142	D6	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
143	C6	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
144	D5	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
145	C5	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
146	D4	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
147	C4	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
148	D3	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
149	C3	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
150	D2	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
151	C2	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
152	D1	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
153	C1	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
154	D0	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
155	C0	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
156	VDDA	PWR		Analogue supply	Not applicable	

Table 3.2.1-1: LQFP156 Pin Table

Class	Description
PWR	Power pin
AI	Analogue input
AO	Analogue output
AIO	Analogue IO
I	CMOS input (no pull up)
Iwpu	CMOS input with weak pull up[2]
O	CMOS push-pull output
ODwpu	CMOS Open drain with weak pull up[2]
OS	CMOS Open source no pull down
OD	CMOS Open drain no pull up
IO	CMOS input/output
IOwpu	CMOS input/output with weak pull up[2]

Table 3.2.1-2: Pin Classes

As a general convention, communication pin names are prefixed with "SLV" or "MST" to designate Slave or Master. Pin names with an "n" at the start of the function name designate an active-low signal e.g. MSTnIRQ is an active low interrupt from the Master. Also note that dual-mode pins are named (A) / (B), where (A) is the applicable name in the first mode and (B) in the second mode.

[2]Pull up/down intended as level keeper only.

4 Pin Descriptions

4.1 GND

The 0V power supply connection. Connect all GND pins to 0V.

4.2 A0..34, B0..2, B31..34, C0..34, D0..34

These are the sense pins, connected to the 2D CTS electrodes. The exact pin to electrode mapping is defined using the TouchHub configuration tool. The routing and layout of the connections to these pins is very important for best performance and is described in a separate application note. See **Appendix B References**.

4.3 VDDA

The analogue sub-system's power supply connection, running at nominally 3.3V. Connect all VDDA pins to 3.3V. The VDDA supply must be low noise and well regulated. Each VDDA pin must have a parallel 22uF and 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. An additional single bulk ceramic, tantalum or electrolytic capacitor of $\geq$ 22uF is required on the VDDA supply. Under most conditions its is acceptable to share this supply with VDDI[3].

These pins have special layout considerations. See **Appendix A.1.3 Layout and Routing Considerations for VDDA tracks** for further details.

4.4 VDDI

The I/O sub-system's power supply connection, running at nominally 1.8V to 3.3V. Connect all VDDI pins to this supply. The VDDI supply is used to define the interface logic level used to communicate with the host, so must be sufficiently well regulated to ensure reliable high speed comms. Each VDDI pin must have a 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. If the VDDA and VDDI supplies are separate, an additional single bulk ceramic, tantalum or electrolytic capacitor of $\geq$ 1uF is required on the VDDI supply. Under most conditions it is OK to share this supply with VDDA, in which case route VDDI as a separate net and use a star point connection to VDDA to help to isolate noise on the two domains[3]. CMOS I/O pins should never exceed the limitations stated in Table 9.1-1 (Vpc and Vpa) during power up, operation or power down.

These pins have special layout considerations. See **Appendix A.1.3 Layout and Routing Considerations for VDDA tracks** for further details.

4.5 SLVnIRQ

The device generates an interrupt whenever it has a report waiting to be read by the host. The slave interrupt pin asserts low in this case. It returns to a Hi-Z state when no reports are pending (but is weakly pulled up). The action of the host reading a report is to consume that report, and when all reports have been consumed the pin returns to Hi-Z (wpu). In order to affect an acceptably fast low-to-high transition in the presence of parasitic capacitance, an external pull up of 1K to 10K is required. The host device should use *level* triggering to sense the interrupt.

4.6 SLVSDA / SCK

This pin serves different functions depending on the communication mode selected by the nSLVI2C pin:

Slave I^{2}C Mode: The pin serves as the I^{2}C Data pin to connect to the host. It has a weak internal pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.
Slave SPI Mode: This pin becomes the SPI SCK clock input from the host. In this mode no additional pull-up resistor is required.

[3] Assuming the I/O level is 3.3V.

4.7 SLVSCL / nSS

This pin serves different functions depending on the communication mode selected by the nSLVI2C pin:

Slave I²C Mode: This pin is the I²C Clock pin to connect to the host. It has a weak internal pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.
Slave SPI Mode: This pin becomes the SPI active low Slave Select input from the host. In this mode no additional pull-up resistor is required.

4.8 SLVI2CADDRSEL / MOSI

This pin serves different functions depending on the communication mode selected by the nSLVI2C pin:

Slave I²C Mode: Selects between 2 addresses for the device. See **7.3.1 Slave Address Selection** for details. The pin includes a weak pull up. It is strongly recommended to terminate this pin directly to GND or VDDI (as required) to completely override this pull up (but only when in Slave I²C mode!).
Slave SPI Mode: The pin becomes the MOSI input from the host.

4.9 nSLVI2C / MISO

This pin serves different functions depending on its state as sampled at power-on or reset:

Sampled low at reset: Selects Slave I²C communications mode. The pin includes a weak pull up. It is strongly recommended to terminate this pin directly to GND to select Slave I²C mode.
Sampled high at reset: Selects Slave SPI communications mode. The pin includes a weak pull up. It is strongly recommended to use a supplemental pull-up of 1K to 10K to select SPI mode; the pin must not be terminated directly to VDDI ! On switching to SPI mode, the pin is changed to an output driver and is used as the MISO output to the host.

4.10 DNC

Do not connect. This pin has an internal connection to the device and must not be connected externally.

4.11 GPIO0..4

General purpose I/O pins that can be configured and used by the host as required. Each one has an internal weak pull up included. Note the optional use of GPIO1 as an HSYNC input and GPIO2 as a VSYNC/EXTSYNC input (these optional selections are made via the device's configuration registers).

4.12 DNC

Do not connect. This pin has an internal connection to the device and must not be connected externally.

4.13 nRESET

This pin is the asynchronus master hardware reset. Asserted low it returns the device to its reset state. When high, the device operates as normal. The pin has a weak internal pull up which must be supplemented with a 1K to 5K pull up and optionally a 10nF ceramic bypass capacitor to GND[4] (to offer the best fast-transient immunity in harsh EMI applications).

[4]Check the ability of the connected reset driver to support this capacitive load.

4.14 VDDC

The core sub-system's power supply output, driven by an internal LDO running at nominally 1.8V. If there is more than one VDDC pin then connect them all together to form a single net. Each VDDC pin must have a parallel 22uF and 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. No other connections to the VDDC net are permitted.

These pins have special layout considerations. See **Appendix A.1.3 Layout and Routing Considerations for VDDA tracks** for further details.

4.15 SHIELD2DCTS

The 2D CTS sense pins must be routed using a shielding technique using a dummy electrode that is driven by this pin. This is described in a separate application note. See **Appendix B References**. SHIELD2DCTS must be bypassed to GND near to the device, with a single 1nF 6V ceramic X5R (or tighter tolerance) capacitor.

5 Reference Schematic

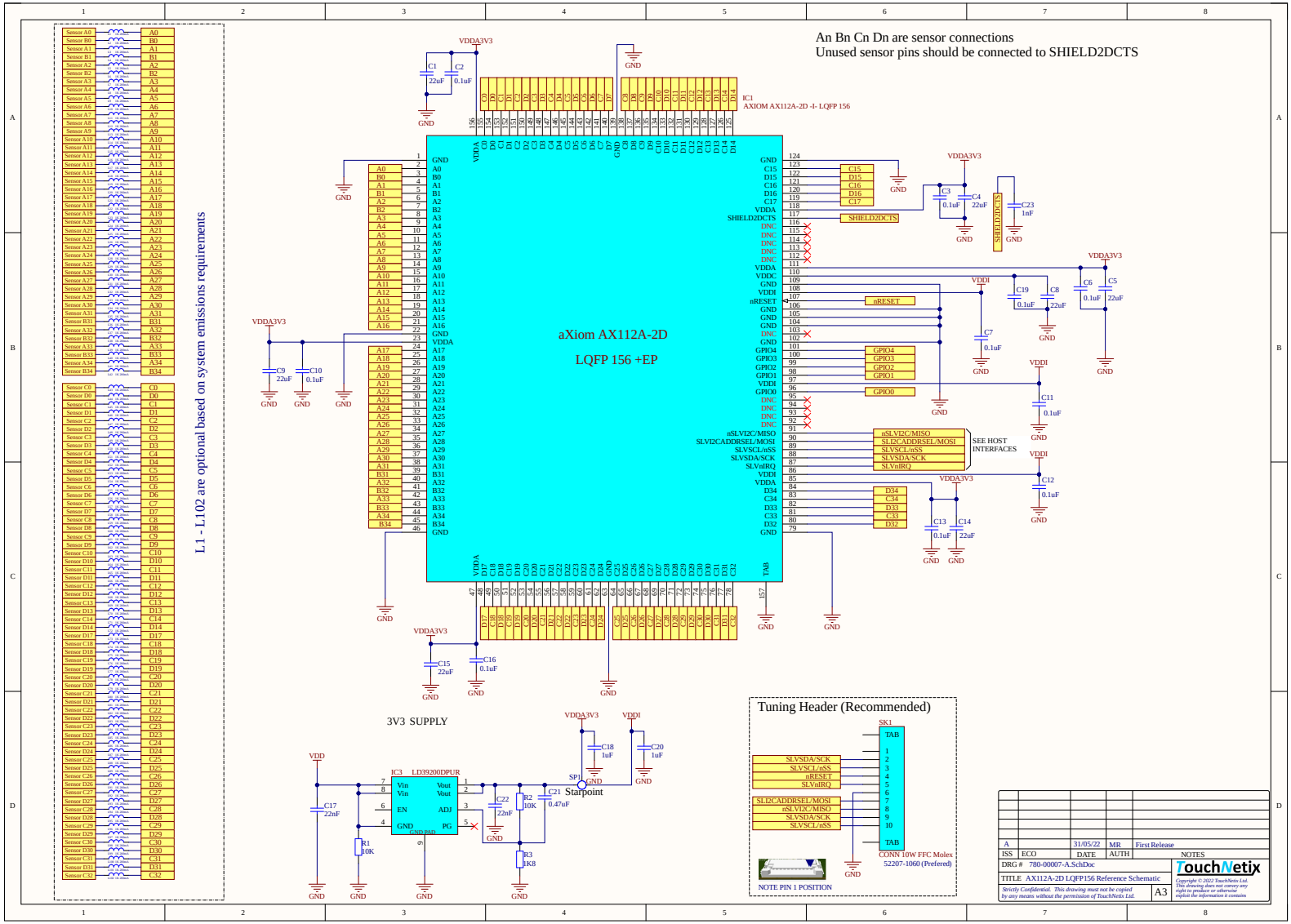

Figure 5-1: Reference Schematic (LQFP156)

6 Sensing

6.1 Sensing Overview

The aXiom sensing architecture has been designed to measure capacitance, with a Signal-To-Noise ratio that goes far beyond existing solutions, whilst also being sympathetic to the diverse range of EMC and EMI challenges that are faced in real-world applications. Using a high purity narrow band drive waveform, with an amplitude of just 1.25V [5], the controller not only has extremely low Radiated Emissions but is also sympathetic to the long term sensor ageing problem, that is seen when operating at elevated temperature and humidity. This little-documented aspect of touch sensors, can only be addressed by using low amplitude DC-neutral drive techniques, to radically slow down the effects of electro-corrosion, electro-migration and e-field induced damage to various metals and some polymeric materials. To pass stringent EMC tests, in particular those dealing with injected currents (Conducted Immunity), many competing controllers resort to high sensor drive amplitudes to improve their overall SNR. While this may be successful in one regard, it seriously compromises both sensor lifetime and Radiated Emissions. Coupled with drive waveforms that are often square in nature (leading to complex harmonic content), it can be seen that a pure low amplitude drive signal is a major advantage in tough environments. To measure capacitance using small signals in the presence of large amounts of external noise, requires that the sensing architecture and the analogue front end of the device, is carefully optimized to be able to recover the carrier, even when this is hundreds of times smaller than the interference; techniques that are well understood in modern radio systems but that are seldom used in touch sensing.

The device can be connected to a broad range of Capacitive Touch Sensor (CTS) styles, including both single and double connected versions of the well known *Diamond*, *Flooded* and *True Single Layer* types. To further extend the range of applications that are possible, the device treats its sensor pins as general resources and is able to use any pin as either drive or sense. This allows great flexibility in the aspect ratio of the CTS sensing area; the pool of sensor pins can be mapped to sensor electrodes in any ratio that is needed. This allows everything from long-thin touch areas to square touch areas to be created easily. The sensing architecture has more than enough dynamic range to handle the sensor measurement, in the presence of the diverse parasitics created by such extreme aspect ratios. This capability further extends to allowing direct support for truncated electrodes, often found in non-rectangular touch applications[6].

The high SNR of the acquisition engine, allows a wide range of glove types and thicknesses to be used with the CTS. Alternatively, high quality multi-touch tracking through very thick plastic cover panels becomes possible; over 10mm of acrylic overlay can be used and can even have varying thickness, thanks to a novel compensation scheme that helps to unify the touch sensitivity across diverse thickness changes. Sensing through small air gaps also becomes viable[7]. Water suppression is built into the device's capability, allowing wet finger tracking and water rejection[8].

[5] 2.5V pk-pk
[6] Imagine a circular sensor; the outer electrodes have almost no surface area compared to those in the middle.
[7] Subject to mechanical stability considerations.
[8] Including saline solutions, blood etc with some sensing compromises.

The acquisition engine makes its measurements during a period called a Frame. Each frame is subdivided into smaller time units called *Slots*. During a Frame, different measurement tasks (Slots) are scheduled. Typically, a Frame consists mainly of CTS and/or CDS Slots, simply because there are so many measurements to take. There are also typically, a small number of Slots used for housekeeping. To simplify things, TouchHub2 can automatically configure the Frame based on the system's requirements.

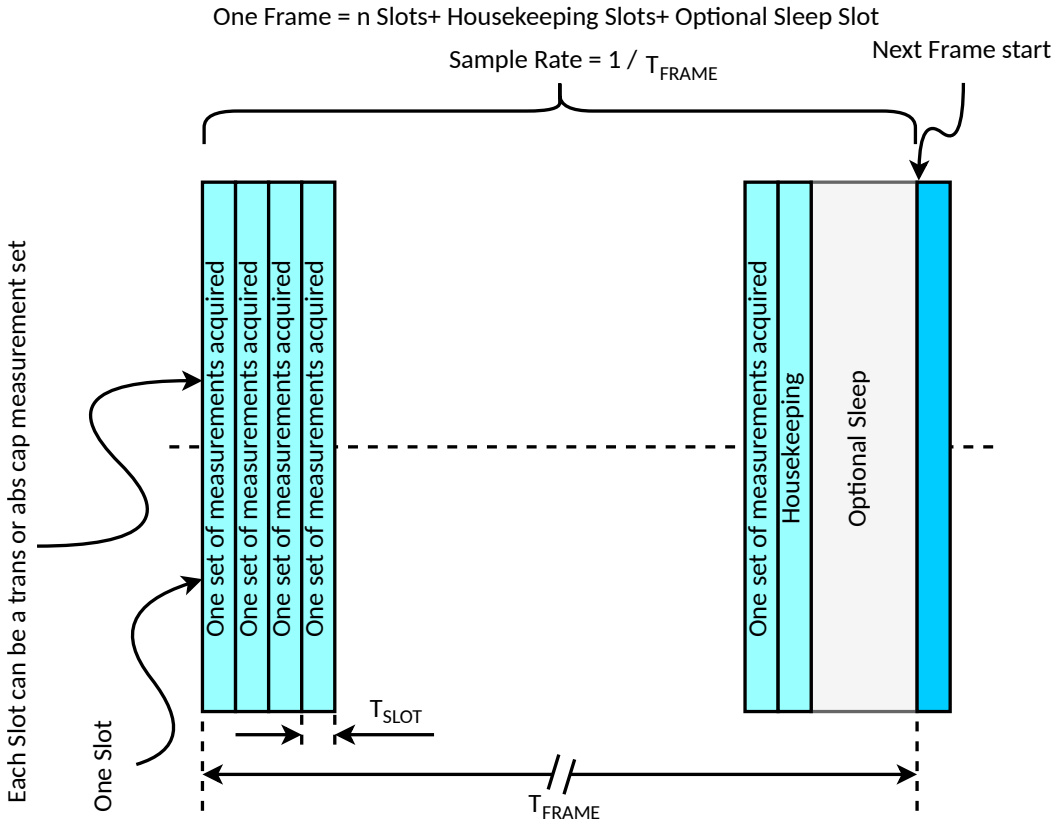

Figure 6.1-1: Acquisition Engine Frame Structure

The overall architecture of the AX112A-2D is shown below in simplified form.

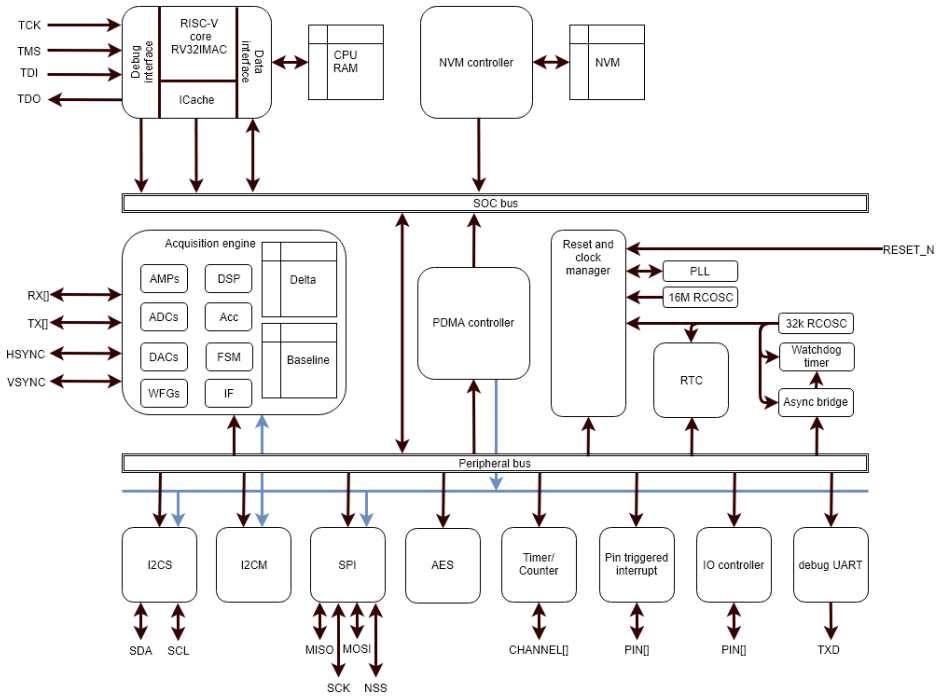

Figure 6.1-2: Simplified System Architecture

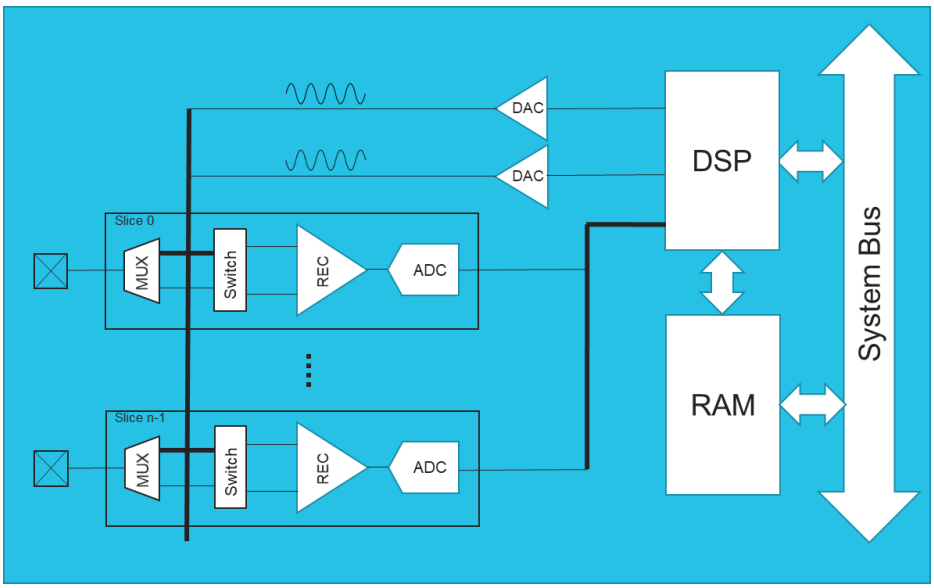

Figure 6.1-3: Simplified Sensing Architecture

6.2 Touch Sensing

The AX112A-2D uses a *transverse capacitive* measurement technique ("trans-cap") to sense the capacitive coupling between pairs of electrodes. Traditionally, these would be called *transmitter* and *receiver* (or *drive* and *sense*) electrodes. The AX112A-2D sensing architecture is more flexible than existing devices, which makes it misleading to think of electrodes as having fixed transmit and receive functions. Rather, any electrode can be either function. Hence, we'll refer to them as either just electrodes or *sense pins* or even sometimes *channels*; the names are freely interchangeable.

The AX112A-2D has 112 sense pins. These can be wired to the electrodes of a 2D Capacitive Touch Sensor (2D CTS) in a very flexible way, enabling the creation of sensing areas with arbitrary aspect ratios. To simplify the design task, the supplied TouchHub2 software can take high-level design requirements, such as the number of electrodes in each axis of the CTS, and automatically decide which device pins to connect to which electrodes. For this reason, when you look in the Pin Description tables you will not see familiar names like "TX0" or "RX10". Instead, you will see pins with more generic names like "A0" and "D3". This way we reduce the risk of inferring the function of these pins. Likewise, we refer to the two axes as Rows and Columns rather than Tx and Rx.

The 2D CTS is typically formed of a grid of orthogonal electrodes. Where a Row and Column electrode intersect, a sensing node is formed. The capacitance of all nodes in the CTS are measured by the device once every *frame*[9]. When a user touches the CTS, the node capacitances change near to the touch position and cause what is referred to as a *touch delta*. It is this touch delta that the device senses and converts into accurate touch positions.

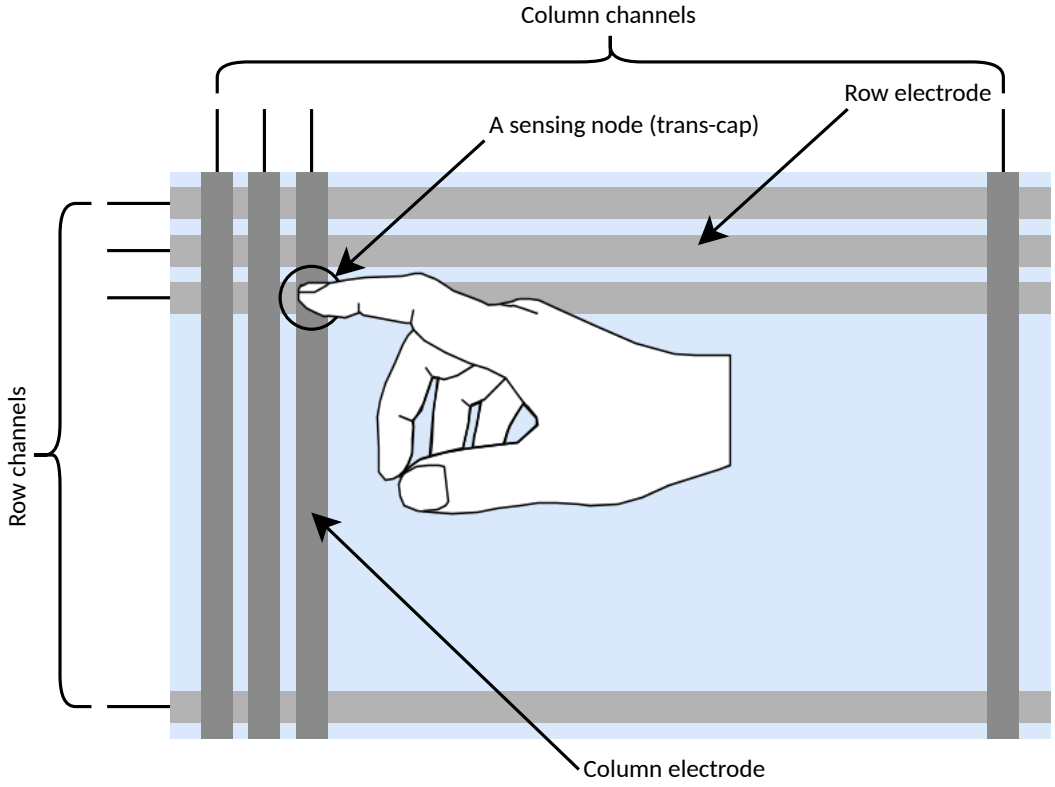

Figure 6.2-1: Channel Naming Convention

[9]The measurement is conducted by the acquisition engine, which is instructed what to do by a configuration *profile* created by TouchHub2.

The AX112A-2D can measure up to 3136 nodes; this means that configurations where (RXs $\times$ TXs $\leq$ 3136) are supported. Some large, almost square, designs may need to limit the number of RX and TX to stay within this limit. While any pin can be configured as either TX or RX, there are multiple factors which affect performance including how electrodes are assigned to pins. Therefore, it is necessary to use the TouchHub2 tool to determine the optimal connections to use for your sensor.

The AX112A-2D can report up to 10 concurrent touches, using advanced signal processing techniques to accurately resolve touch positions at up to 16 bits of resolution. To enhance the rate at which the host can read the status and position of these touches, all 10 touches are combined into a single compact report, reducing communication traffic and reducing the chance of the host missing important touch events.

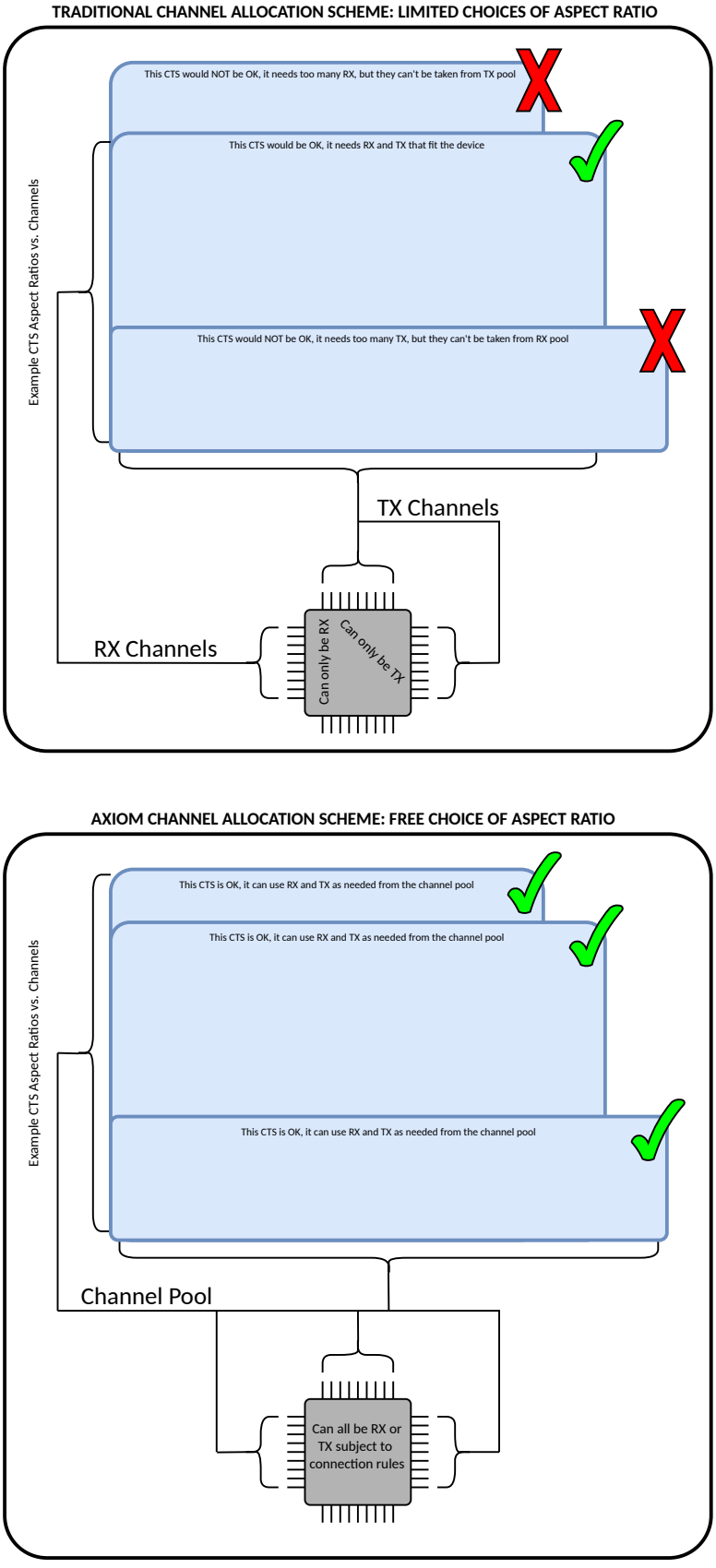

Figure 6.2-2: Traditional vs. aXiom Channel Allocation

6.3 Variable Thickness Lenses

The AX112A-2D 's acquisition engine includes a facility to scale the measured 2D touch delta array on a node-by-node basis. The scaling factors for each node can be changed using TouchHub2 via a configuration file. For most touch controllers, scaling the measured deltas in this way would simply amplify the background noise, to a point where it would cause excessive touch position jitter and even false detections. However, because the SNR of the AX112A-2D is so much higher, this amplification becomes viable, allowing corrections to the apparent gain of each and every node on the 2DCTS.

This delta scaling opens up interesting new possibilities to support cover lenses with widely varying thicknesses across their surface. The scaling allows both attenuation and amplification, giving an adjustment range of x16 between areas requiring the lowest and highest gains. Additionally, any node can be completely suppressed, allowing regions of the sensor to be disabled. The rear side of the lens can remain flat, or perhaps curved in just 1 direction, making production lamination far easier than some schemes, that try to in-mould laminate the touch sensor into complex uniform thickness lenses.

Figure 6.3-1: Example of a Flat Sensor and Variable Thickness Lens

6.4 EMC Features

One of the toughest challenges faced by capacitive touch sensors, is that of achieving high electrical noise immunity to conducted interference. The reason is simple: in most typical electronic systems we only need to worry about noise on the power supplies relative to our own GND (0V), which is local to the system. Excess noise can always be filtered out. In a capacitive touch system, part of the sensing current travels via a capacitively coupled route, through the touching finger and back to the controller *via a 3rd terminal; earth*. So noise that is *common* to power *and* GND relative to earth, will appear in the capacitive measurement when, and only when, a touch is applied. In some compliance tests, this immunity aspect is checked by injecting a *common mode* signal and sweeping it from 150KHz to 80MHz, 80% amplitude modulated. This causes a voltage disturbance of nearly 50V peak-to-peak with respect to earth[10]! Noise of this type is encountered in many industrial, medical and automotive environments, caused by switch mode power supplies, inductive coupling between equipment cables etc. Clearly, because the noise is "earth referred" there is no obvious conventional way to filter it.

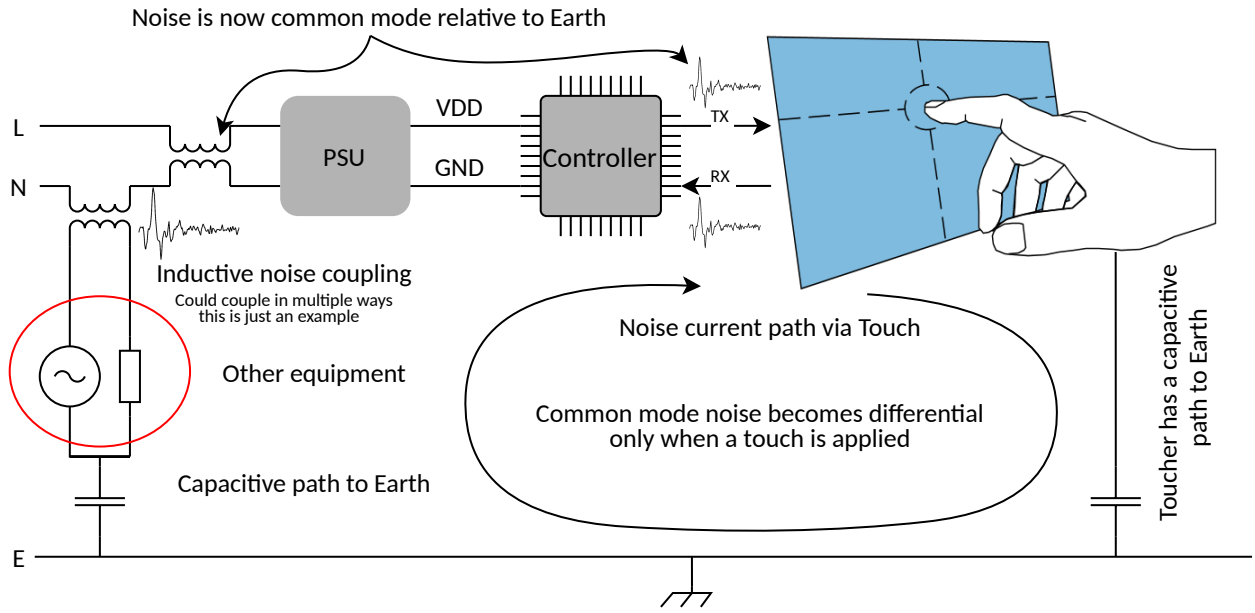

Figure 6.4-1: Example Common Mode Noise From "Other" Equipment

The nature[11] of a typical touch sensor is that capacitance measurements at a frequency between 50 and 500KHz tend to be optimal. Clearly this frequency range overlaps the test band mentioned above; injecting noise at or near the measurement frequency will directly affect the measurement. In order to counter this, the AX112A-2D is frequency agile, being able to move its measurement frequency at will. This is known as *frequency hopping* and is a well understood method for avoiding interference in many aspects of electronics and radio communications[12]. The AX112A-2D uses a very narrow bandwidth to measure capacitance. This has the great advantage that in a congested spectrum with narrow *quiet gaps*, it is still possible to relocate the acquisition frequency to affect low noise measurements. Many competing touch devices use an *integration* technique, employing an integrator with a sampled input. This gives rise to an extremely wide and complex *reception spectrum*[13], making it hard to hop away from interference. A second advantage that narrow band demodulation offers, is that it is possible to very accurately measure the amount of external noise present at any moment; the AX112A-2D does this continuously each frame and hence it can react instantly if noise suddenly appears in the system. Competing systems can sometimes be fooled into thinking that there is zero noise, when certain noise frequencies are injected, and hence their measurements fail when no preventative steps are taken to frequency hop. The AX112A-2D can never be fooled in this way. The AX112A-2D also sets new standards in its ability to maintain several internal operating points, allowing it to hop quickly and seamlessly between frequencies.

[10] e.g. EN61000-4-6 Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields: Level 3.

[11] i.e. its -3dB frequency response.

[12] Invented c. 1942 for guided torpedo anti-jamming.

[13] the sampling window imposes a $\frac{sin(x)}{x}$ frequency response characteristic which is full of slowly reducing lobes and few, very narrow gaps to hop to.

To further protect the AX112A-2D against EMI, the signal path in the analogue front end, uses techniques to avoid its amplifiers from over-ranging in the presence of very high levels of interference. Even when such countermeasures are employed, the touch report stability is still industry leading, thanks to the high SNR of the acquisition engine.

So far we have talked only about immunity to interference, but in some applications, emissions are just as big an issue. The AX112A-2D drives the sensor with a pure 1.25V amplitude sinusoidal waveform at a single frequency. Compare this to many competing devices that drive the sensor using a square wave at up to 30V peak-to-peak, leading to problems when trying to pass emissions certification.

6.5 Water Suppression

The AX112A-2D employs a unique architecture that allows it to make two types of measurement during the same frame: i) trans-cap (as already discussed) and ii) a second measurement type called *absolute capacitance* or *abs-cap*. Abs-cap measures the total capacitance of an electrode, rather than the coupling capacitance to another electrode. When abs-cap measurements are taken, they are done concurrently on a whole group of electrodes. This means that multiple electrodes are driven with near identical waveforms and hence the coupling capacitance from neighbour to neighbour is virtually neutralized; only the total capacitance of each electrode to GND+earth is sensed. This has the useful side-effect that water puddles, laying on the CTS lens surface that bridge between/across electrodes, become almost invisible from a capacitance point of view. Trans-cap measurements, on the other hand, will see normal touches and water puddles as almost identical. By making two types of measurement, the AX112A-2D can discriminate between such contacts and hence can offer a great improvement in *waterproofing* the overall touch solution.[14]

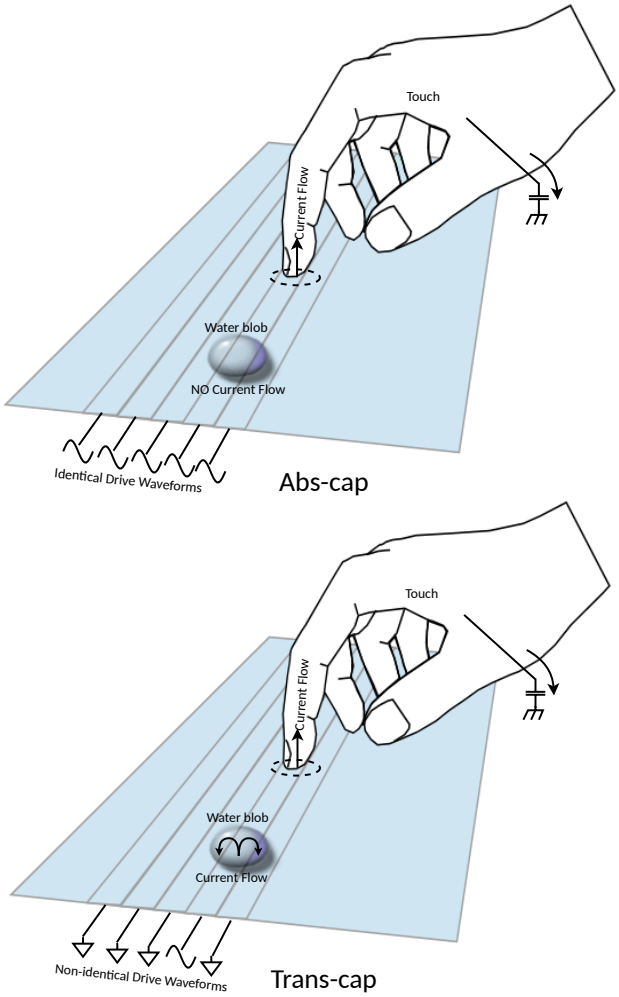

Figure 6.5-1: Different Behaviors With Abs-cap and Trans-cap Measurements With Water and Touch

[14]These effects have been well known since the late 90's but implementation of dual measurement-mode controllers only became popular with the growth of mobile devices.

Abs-cap measurements come with their own set of challenges, mainly caused by the fact that the change in capacitance with touch, is a much smaller proportion of the electrode's *baseline capacitance* than it is with trans-cap[15]. This leads to a requirement for even greater measurement SNR. There are ways to mitigate some of the extra capacitive loading on the electrodes, particularly those that live at the edges of the CTS, that would normally be exposed large areas of GNDed conductor (e.g. other traces, ESD rings etc). See **Appendix B References** for links to application notes that cover this topic in more detail.

During a frame, the AX112A-2D typically measures a 2DCTS in trans-cap mode across many sub-frame time slots (See **6.1 Sensing Overview)**. Additionally, it will use multiple slots to measure the CTS in abs-cap mode. TouchHub2 software can create a configuration file that will schedule all of these measurements automatically.

[15]i.e. the touch delta percent is smaller because the baseline capacitiance is so much higher (perhaps 10 to 100 times that of a trans-cap node).

6.6 Sensor Compatibility

The wide measurement range of aXiom devices means they can operate with most sensor styles and constructions. For further details refer to **TNxAN00042 aXiom Touch Controller Sensor Compatibility**.

6.7 Sensor Protection

Touch sensors are fabricated using a range of materials, some of which are extremely stable and some of which are not. Indium Tin Oxide (ITO), for example, commonly used to make the sensor's electrodes, is a ceramic conductor[16] that is remarkably robust to environmental damage caused by high temperature and humidity. It is very common to leave ITO exposed to the environment, even in harsh conditions[17]. Other materials, notably the Silver commonly used to form the edge wiring on sensors, is a very different proposition when exposed to such conditions and when it is also supporting a voltage difference to a neighbouring conductor. In these conditions, an effect known as Electro-Migration can occur over time, that forms small conductive "dendrites" between traces that eventually short-circuit the touch sensor channels and cause premature failure. This is true for sensors that are fabricated on glass or plastic substrates. A common requirement in industrial and automotive environments, is to achieve a 504 hour operating life when exposed to 60°C and 90% relative humidity. This requirement sounds easy enough and indeed, many claim that their sensor/controller combination can pass this test. The reality is that the test is often conducted like a "storage" test with no power applied during the environmental exposure. This is *not* the same test! It is the application of power, and hence voltage, that causes the Electro-Migration. The rate of migration depends on many factors including the voltage differential between traces.

For this reason, the AX112A-2D takes two special precautions:

1. It uses a very small drive amplitude of 1.25V (2.5V pk-pk) to measure the capacitance. Compare this to controllers that use 10V to 30V to drive the sensor.
2. It also biases all inactive electrodes in such a way that, all active drive voltages swing symmetrically either side of this bias; this has the effect of further slowing migration as the net DC level is approximately zero[18]. Compare this to controllers that bias inactive electrodes to GND and drive with a pulsed 30V waveform.

Further discussion of these effects are beyond the scope of this document, but further information can be found in **Appendix B References**.

[16] It can also be classed as an alloy depending on its exact composition.
[17] Noting that standing water or other contaminants can etch ITO if they are acidic in nature.
[18] Refered to as a DC neutral drive.

7 Host Interfaces

7.1 Available Interfaces

The AX112A-2D offers two ways to communicate with the host;

1. A slave I²C interface, consisting of the following pins (taking the name **before** the "/"): (**SLVSDA / SCK**), (**SLVSCL / nSS**) and an interrupt (**SLVnIRQ**). Rates up to 400KHz are supported.
2. A slave SPI interface, consisting of the following pins (taking the name **after** the "/"): (**SLVI2CADDRSEL / MOSI**), (**nSLVI2C / MISO**), (**SLVSDA / SCK**), (**SLVSCL / nSS**) and an interrupt (**SLVnIRQ**). Rates up to 4MHz are supported.

7.2 Mode Selection

A single pin controls which host interface is selected: **nSLVI2C / MISO**. The pin is sampled as the device starts up (from a power on, or reset event):

If the pin is sampled low, **Slave I²C** mode is selected.
If the pin is sampled high, **Slave SPI** mode is selected.

The pin includes a weak pull-up that must be overridden either by tying it to GND, (for I²C mode) or by **pulling up** with a supplemental resistor to VDDI (for SPI mode)[19] (see **4.9 nSLVI2C / MISO**).

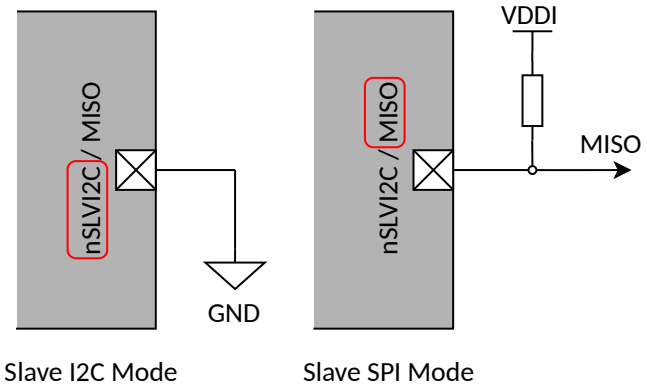

Figure 7.2-1: Communication Mode Selection

[19] In SPI mode the pin changes to become an output and hence must **not** be pulled up by tying directly to VDDI.

7.3 Slave I²C Mode

7.3.1 Slave Address Selection

Two different Slave I²C addresses can be selected with the **SLVI2CADDRSEL / MOSI** pin. The pin is sampled as the device starts up (from a power-on, or reset event):

SLVI2CADDRSEL / MOSI level	Slave I²C Address (7-bit hex)
low	0x66
high	0x67

Table 7.3.1-1: Slave I²C Address Selection

See **4.8 SLVI2CADDRSEL / MOSI** for notes on terminating this pin.

7.3.2 Connections

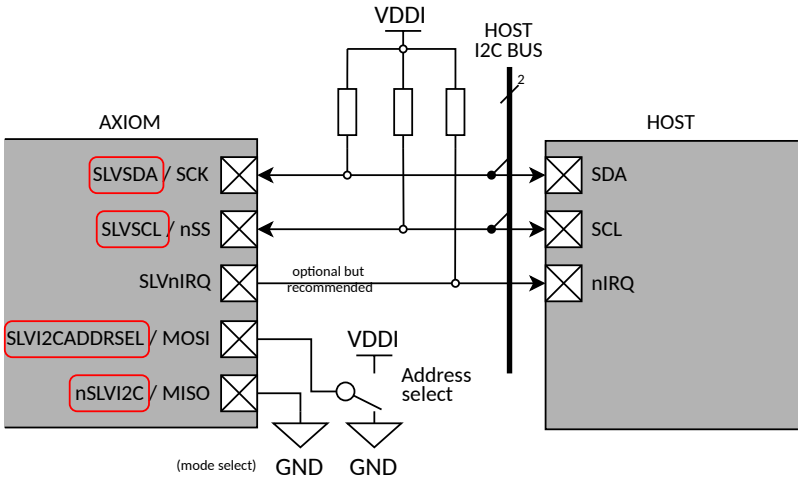

Figure 7.3.2-1: Slave I²C Connections

7.3.3 I²C Protocol

The communications protocol used to access configuration registers in the device and to receive event reports from the device, can be found in **TNxAN00035 aXiom Touch Controller Comms Protocol**. Real-time report collection from the device over the I²C interface, has been optimized to work in an interrupt driven mode rather than being polled.

7.4 Slave SPI Mode

7.4.1 Device Selection

In order to communicate with the device, the **SLVSCL / nSS** pin must be asserted low for (at least) the duration of the communication. It is OK to permanently connect **SLVSCL / nSS** to GND when in SPI mode, if the AX112A-2D is the only device on the SPI bus.

7.4.2 Connections

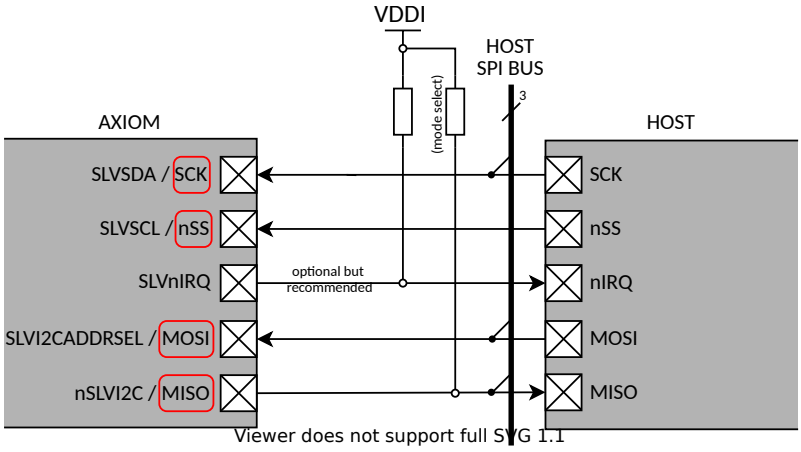

Figure 7.4.2-1: Slave SPI Connections

7.4.3 SPI Protocol

The SPI interface operates in Mode 0[20]. The communications protocol used to access configuration registers in the device and to receive event reports from the device, can be found in **TNxAN00035 aXiom Touch Controller Comms Protocol**. Real-time report collection from the device over the SPI interface has been optimized to work in an interrupt driven mode rather than being polled.

[20] Clock Polarity:0, Clock Phase:0, Clock Edge:1 (Clock idles at 0, and uses rising edge to sample data, and uses falling edge to shift data).

8 Programming Model

aXiom devices use a register interface called *Touch Controller Protocol*, or TCP, which defines each and every register in the device, how they are organized and accessed. TCP covers configuration and tuning registers, as well as general status and information registers. For the transport of "live" data, TCP also describes a reporting scheme; this is particularly important for host device drivers, because it is the mechanism by which the device sends real-time touch information to the host.

While all aXiom devices use TCP, the exact set of registers and features offered by a specific device do vary. Hence, this general document does not present a detailed programming interface. Instead, you are directed to **TNxAN00038 aXiom AX112A Touch Controller Programmer's Guide**.

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The runtime firmware in aXiom devices is field upgradable using a command and register interface called "Bootloader Protocol" or BLP, details of which can be found in **TNxAN00043 aXiom Touch Controller Bootloader**.

9 Device Characteristics

All quoted ranges are at an operating ambient temperature of 25°C unless otherwise stated.

9.1 Absolute Maximum Ratings

Stresses beyond those listed in Table **9.1-1** may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these, or any other conditions beyond those indicated in **9.2 Operational Ratings** is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	*Parameter*	*Min*	*Max*	*Units*
VDDA	Analogue supply	-0.3	4	V
VDDI	I/O supply	-0.3	4	V
V_{pc}	Voltage applied to any CMOS pin	-0.5	VDDI+0.5	V
I_{pc}	Maximum source/sink current for any CMOS pin	-25	25	mA
V_{pa}	Voltage applied to any Analogue pin	-0.5	VDDA+0.5	V
I_{pa}	Maximum source/sink current for any Analogue pin	-25	25	mA
T_S	Storage temperature (non operating)	-65	150	°C
T_J	Junction temperature (operating)		125	°C
ESD_{hbm}	ESD rating, human body model[21]		2000	V
ESD_{cdm}	ESD rating, charged device model[21]		750	V

Table 9.1-1: Absolute Maximum Ratings

[21] Discharge direct to device pins. Discharge rating to the sensor/lens in a system is application specific but is typically far higher than this device rating.

9.2 Operational Ratings

9.2.1 Operating Conditions

Symbol	*Parameter*	*Range*	*Units*
T_A	Ambient temperature[22]	-40 to +105	°C
RH_A	Ambient relative humidity (non-condensing)	10 to 90	%RH

Table 9.2.1-1: Operating Conditions

9.2.2 Power Requirements

Symbol	*Parameter*	*Range*[23]	*Units*
VDDA	Analogue supply	2.97 to 3.63	V
VDDI	I/O supply	1.62 to 3.63	V
IDDA	Active analogue supply current (average over frame)	200 to 250	mA
IDDI	I/O supply current (average over frame)	0.005 to 5	mA
N_{VDDA}	Allowable peak-to-peak noise and ripple on analogue supply	85	mV
N_{VDDI}	Allowable peak-to-peak noise and ripple on I/O supply	200	mV

Table 9.2.2-1: Power Requirements

Note that IDDA varies depending on the device's configuration, which defines the measurement types and durations that are performed. For host power supply sizing and thermal calculations, the maximum stated value should be used as an average, with an allowance for +/-25% current variation away from the average during a measurement frame. The chosen regulator must be able to cope with this transient current behaviour. Generally, a device configuration that employs only Trans Cap measurements, will consume considerably less than one which also enables Abs Cap measurements, that last for a significant percentage of the total frame time.

Also note that IDDI varies significantly depending on the amount of IO activity, but is generally far smaller than IDDA. As noted in **4 Pin Descriptions** VDDA and VDDI are commonly shared and so this current should be added to the overall supply current budget.

9.2.3 Power Sequencing

There are no power sequencing requirements for the application or removal of (or between) VDDA and VDDI. Internal brown-out detection will prevent the device from operating, until both VDDA and VDDC (internal) are properly established. VDDI is not level checked as it does not directly impact the internal operation of the device[24].

CMOS I/O pins should never exceed the limitations stated in Table **9.1-1** (Vpc and Vpa) during power up, operation or power down.

During power-up, while the power rails are stabilising, the voltage levels on the I/O pins may be undefined and should not be relied upon for deterministic behaviour.

9.2.4 Startup Time

From the rising edge of **nRESET** (or when **VDDA** rises above approx. 2V) to the falling edge of **nIRQ**[25]: < **110ms** typical. At this point the device is fully operational.

[22] Subject to appropriate PCB design.
[23] Treat these values as bounding limits
[24] ...but clearly VDDI needs to be correctly established in order to communicate with the device.
[25] The first interrupt is created by a "hello" System Manager report to the host.

9.2.5 Reduced Power Mode

To conserve power during periods of low activity, the device can be configured to enter[26] a Reduced Power Mode (RPM). This trades off first detection latency (from RPM) against power consumption. Typical power reductions of 2 to 6x are possible, as the RPM measurement rate is reduced. For further details refer to **TNxAN00061 aXiom Touch Controller Reduced Power Mode**.

[26] Either automatically or by command.

9.2.6 CMOS I/O Characteristics

Symbol	*Parameter*	*Range*	*Units*
V_{IL}	Logic low input @ 1.8V VDDI	-0.3 to 0.63	V
V_{IH}	Logic high input @ 1.8V VDDI	1.2 to 3.6	V
V_{OL}	Logic low output @ 1.8V VDDI, 1.5mA sink	0.5 max	V
V_{OH}	Logic high output @ 1.8V VDDI, 1.5mA source	1.4 min	V
R_{WPU}	Weak pull up resistance @ 1.8V VDDI (where applicable)	69 - 201	KΩ
I_{IL}	Input leakage current	±1 max	uA

Table 9.2.6-1: CMOS I/O Characteristics (1.8V)

Symbol	*Parameter*	*Range*	*Units*
V_{IL}	Logic low input @ 3.3V VDDI	-0.3 to 0.8	V
V_{IH}	Logic high input @ 3.3V VDDI	2.0 to 3.6	V
V_{OL}	Logic low output @ 3.3V VDDI, 4mA sink	0.5 max	V
V_{OH}	Logic high output @ 3.3V VDDI, 4mA source	2.4 min	V
R_{WPU}	Weak pull up resistance @ 3.3V VDDI (where applicable)	34 - 74	KΩ
I_{IL}	Input leakage current	±1 max	uA

Table 9.2.6-2: CMOS I/O Characteristics (3.3V)

9.2.7 Slave I²C Characteristics

The AX112A-2D implements a Slave I²C interface that is compliant with industry standards. It supports both Standard-mode (100KHz) and Fast-mode (400KHz). Addressing is 7-bit. Clock stretching support by the host *is* required.
Bus timings are as per **UM10204 I²C-bus specification and user manual Rev. 6 — 4 April 2014**. The general form of an I²C transaction is shown below. Additional I/O and timing parameters can be found in the aforementioned document in Table 9 and Table 10.

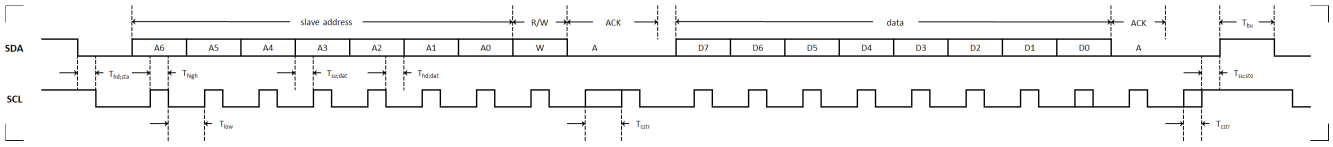


Figure 9.2.7-1: Typical I²C Transaction and Parameters

Symbol	*Parameter*	*Min*	*Max*	*Units*
$T_{hd;sta}$	Start bit hold time	600	-	ns
T_{high}	Clock high period	600	-	ns
T_{low}	Clock low period	1300	-	ns
$T_{su;dat}$	Data setup time	250	-	ns
$T_{hd;dat}$	Data hold time	0	-	ns
T_{cstr}	Maximum clock stretch by slave	-	5	us
$T_{su;sto}$	Stop bit setup time	600	-	ns
T_{bu}	Bus free time between stop and start	1300	-	ns

Table 9.2.7-1: Timings

9.2.8 Slave SPI Characteristics

The AX112A-2D implements a Slave SPI interface that is compliant with industry standards. It supports Mode 0 communication at up to 4MHz. The most significant bits of 8-bit data fields are exchanged first.

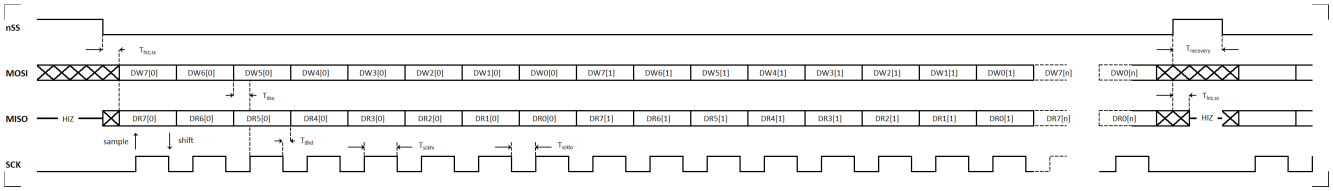


Figure 9.2.8-1: Typical SPI Transaction and Parameters

Symbol	*Parameter*	*Min*	*Max*	*Units*
$T_{hiz;ss}$	nSS transition to MISO transition to/from HiZ	-	20	ns
T_{dsu}	Data setup time (MOSI to SCK)	20	-	ns
T_{dhd}	Data hold time (SCK to MISO)	50	-	ns
T_{sckhi}	SCK high period [27]	100	-	ns
T_{scklo}	SCK low period[28]	100	-	ns
$T_{recovery}$	Slave recovery time, ready for next transfer[29]	-	45	us

Table 9.2.8-1: Timings

[27] Subject to maximum SCK frequency of 4MHz.
[28] Subject to maximum SCK frequency of 4MHz.
[29] The host must ensure that it does not violate this recovery time by ensuring that transfers are spaced apart sufficiently to let the slave prepare for the next transfer. Violating this timing will result in undefined Slave behaviour, possibly lasting beyond the initial violated transfer.

9.2.9 Capacitance Ranges and Drive Limits

Symbol	*Parameter*	*Absolute min*	*Recommended min*	*Recommended max*	*Absolute max*	*Units*
F_{EXC}	Excitation frequency	50	100	500	1000	KHz
$V_{EXC-TRANS}$	Trans Cap excitation voltage pk-to-pk (centered around VDDA/2)	0	2.5	2.5	VDDA-0.6	V
$V_{EXC-ABS}$	Abs cap excitation voltage pk-to-pk (centered around VDDA/2)	0	2.4	2.4	VDDA-0.9	V
$C_{SHIELD2DCTS}$	Total capacitance to GND on SHIELD2DCTS	-	-	-	20	nF
$C_{SHIELDAUX}$	Total capacitance to GND on SHIELDAUX	-	-	-	20	nF
$C_{ABCD-TRANS}$	Total Trans Capacitance load on only A, B, C or D pin	0.5	1.25	2.5	5	pF
$C_{ABCD-ABS}$	Total Abs Capacitance to GND on only A, B, C or D pin	20	-	200	500	pF
$C_{AUX-ABS}$	Total Abs Capacitance to GND on only AUX pin	20	-	-	1000	pF

Table 9.2.9-1: Capacitance Ranges and Drive Limits

Note that F_{EXC}, $V_{EXC-TRANS}$, $V_{EXC-ABS}$ can be directly controlled via the device's configuration registers, so ensuring that the limits are met by tuning. The capacitance limits relate to external factors arising from the attached sensor and associated tracking.

9.2.10 Non-volatile Memory Characteristics

Symbol	*Parameter*	*Range*	*Units*
N_{EC}	Number of erase cycles	10000	cycles
t_{DR}	Data retention @ 85°C T_A	10	years
EDAC	Error detection and correction	Detect and correct all 1-bit errors Detect all 2-bit errors	-

Table 9.2.10-1: Non-volatile Memory Characteristics

9.2.11 Device BIST Capabilities

- RAM self tests.
- NVM EDAC (see **9.2.10 Non-volatile Memory Characteristics**).
- Code execution protection using Watchdog Timer clocked by separate internal oscillator.
- Checksum over NVM.
- Checksum over volatile configuration.
- Checksum over non-volatile configuration.
- Out of range VDDA detection.
- Out of range Acquistion Engine reference capacitor checks.
- Interrupt pin test.
- Cross-check main CPU and RTC/watchdog oscillators against each other.
- Configurable "Heartbeat" report to host allows BIST trigger (limited range) and live status plus, a cross check of the timing period/CPU main oscillator rate.

9.2.12 Sensor BIST Capabilities

- All sense channels allow detection of CTS and CDS impedance leakage of up to 200KΩ to any net.
  - Test can be triggered by host command and optionally run at device boot-up.
- Detection of opens on CTS and CDS electrode channel by configurable signal limits.
  - Test can be triggered by host command and also run periodically using Heartbeat tick.
- Separate signal limit tests for Trans Cap, Abs Cap and AUX.
- Separate test limits for the middle, edges and corners of a CTS (Trans Cap mode) to improve fault coverage.

9.2.13 2D CTS Diagonal Size Range Guide

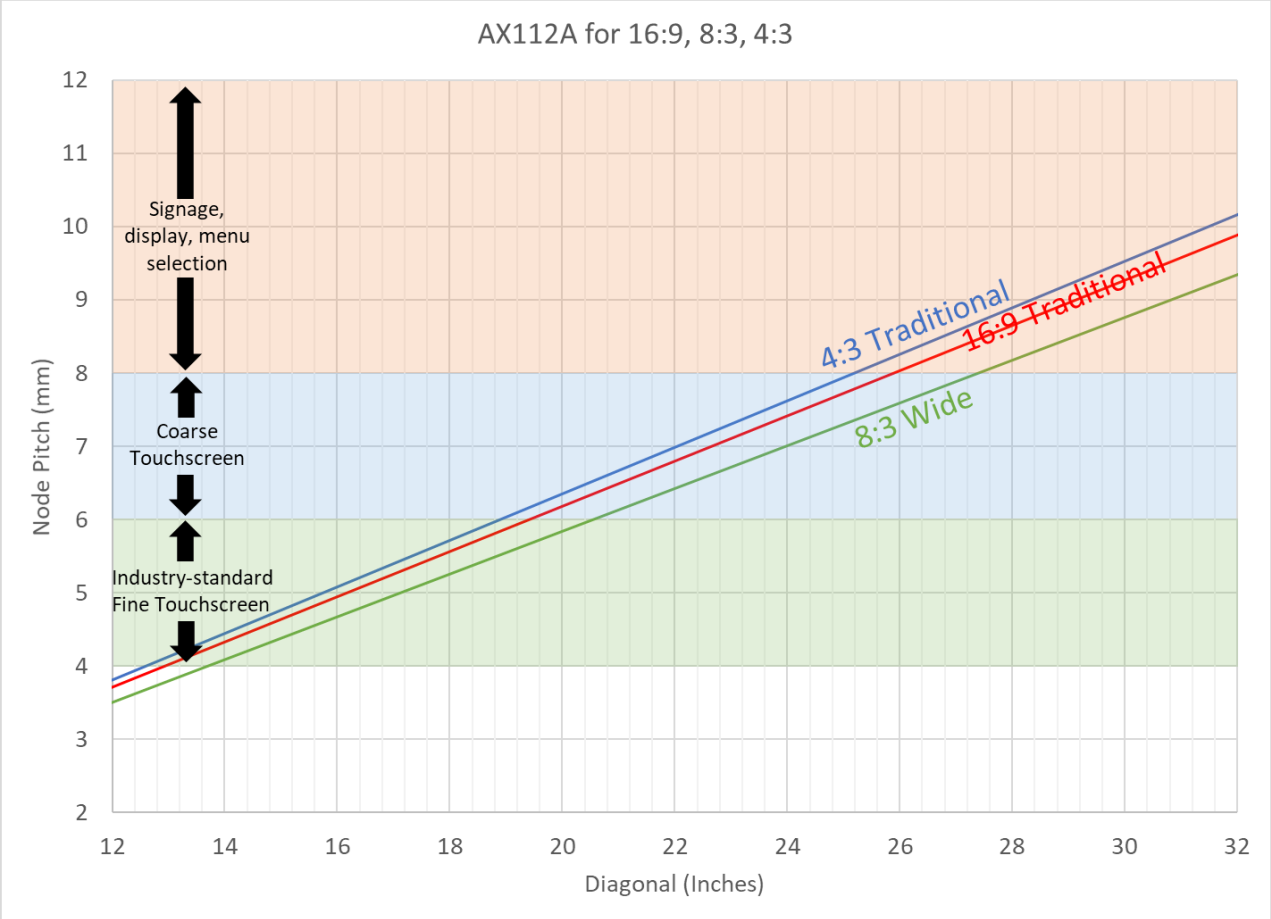
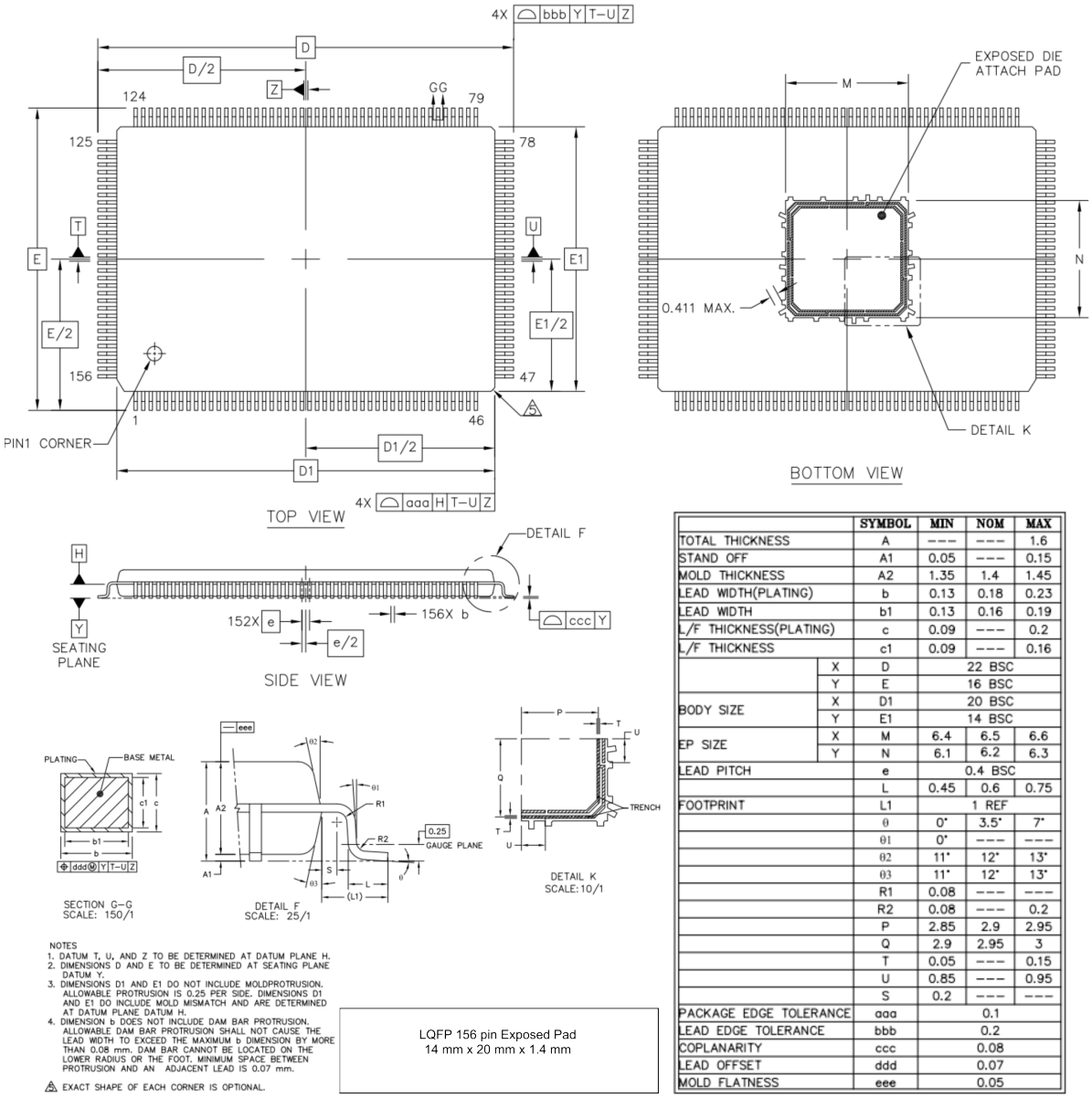


Figure 9.2.13-1: 2D CTS Diagonal Size Range Guide

Appendix A Package Drawings

A.1 LQFP156-EP14201404

A.1.1 Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	22 BSC		
	Y	E	16 BSC		
	X	D1	20 BSC		
	Y	E1	14 BSC		
EP SIZE	X	M	6.4	6.5	6.6
	Y	N	6.1	6.2	6.3
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		P	2.85	2.9	2.95
		Q	2.9	2.95	3
		T	0.05	---	0.15
		U	0.85	---	0.95
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

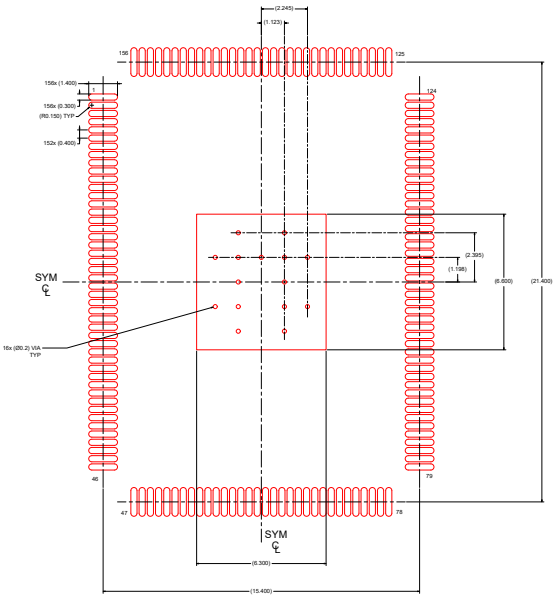
NOTES
1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

⚠ EXACT SHAPE OF EACH CORNER IS OPTIONAL.

LQFP 156 pin Exposed Pad
14 mm x 20 mm x 1.4 mm

Figure A.1.1-1: Package Drawing

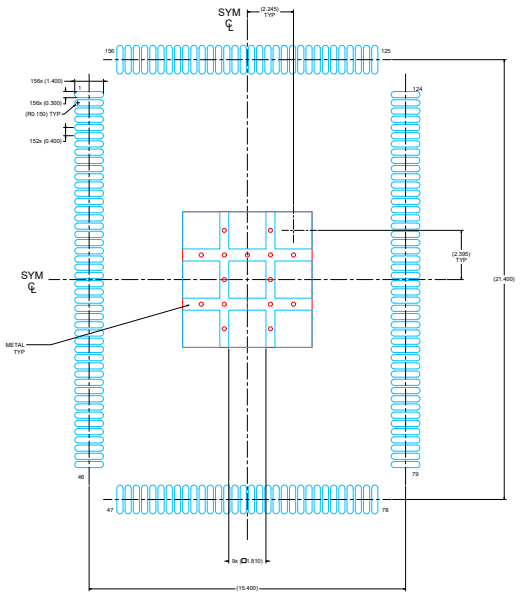
A.1.2 Footprint Information



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN

NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED (NON PREFERRED)



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

FOR REFERENCE ONLY

Figure A.1.2-1: Footprint Drawing

A.1.3 Layout and Routing Considerations for VDDA tracks

To maximize SNR performance, special care must be taken when laying out VDDA power traces.

The maximum tolerated voltage drop *between* VDDA pins varies. The table(s) below should be used for estimation of device current consumption into each pin to allow calculation of the (I*R) voltage drops in your PCB layout. You must then check that they are within the allowed range as listed below.

Pin	Type	Max Current (mA)	ΔV
23	VDDA	30	<2mV ΔV between these pins
47	VDDA	50	
156	VDDA	50	
85	VDDA	5	<5mV ΔV from other VDDA power pins
111	VDDA	200	<5mV ΔV from other VDDA power pins
118	VDDA	5	<5mV ΔV from other VDDA power pins

The images provided are for general guidance. Gerber files for reference designs can be provided by TouchNetix on demand.

Please note: any reference material provided shall be taken as guidance only. PCB designers must ensure to run power/current analysis on their designs to make sure they are compliant with the requirements outlined above.

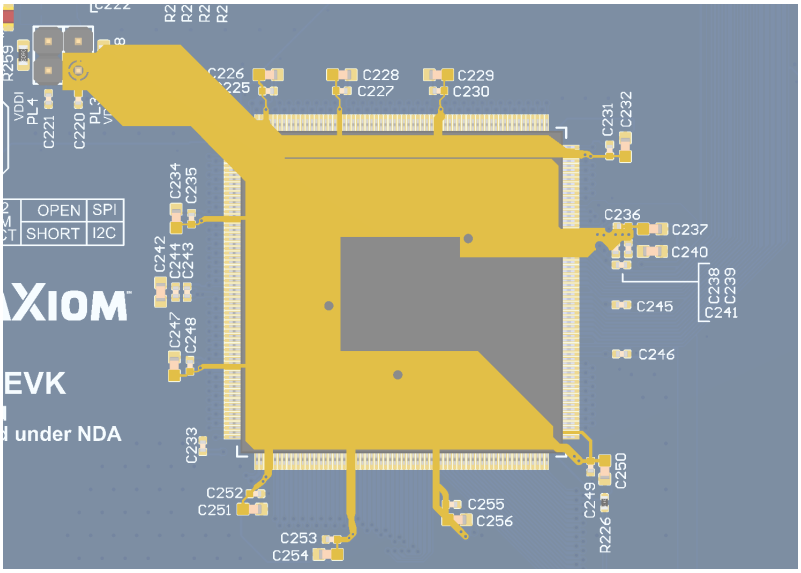


Figure A.1.3-1: C-shaped power routing, balanced amongst all VDDA pins. Figure shows an AX198A, same advice can be applied to this device.

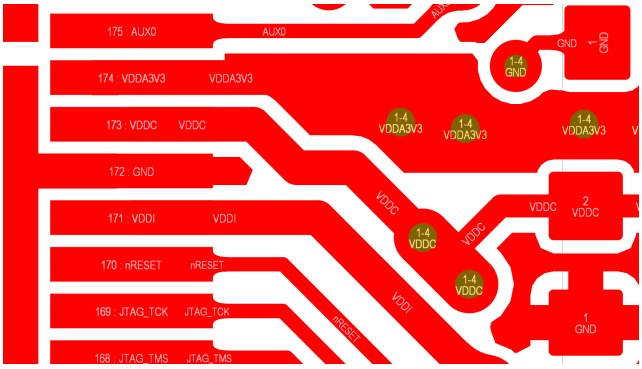


Figure A.1.3-2: Note the use of the widest possible tracking and multiple vias for all VDD tracks. Figure shows an AX198A, same advice can be applied to this device.

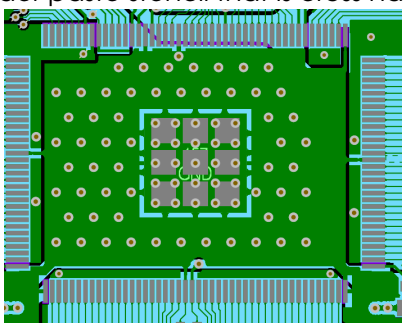
A.1.4 Package Thermal Characteristics

θ_{JA} (junction to ambient [30]) : **21.5**oC/W.

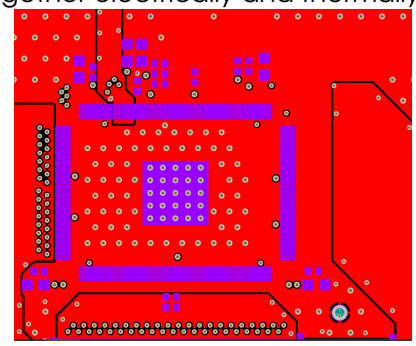
A.1.5 PCB Footprint Notes

The LQFP156 package has an exposed centre GND pad that must be soldered and via'd to suitable copper regions on a 4-layer PCB to help improve the thermal conductivity from junction to ambient. Follow these rules to achieve the stated thermal performance:

1. Use a centre GND PCB pad (to connect to device's exposed pad) which is 6mm x 6mm, using a solder paste stencil that is cross hatched (e.g. 1.5mm square pads) to avoid excessive solder.



2. The centre pad must have a minimum of 25 off, 0.3mm diameter, plugged[31] vias connecting to GND floods on the layers below.
3. Signal traces should not be routed under the device body, to allow maximal copper flood under the device body, without adding capacitive burden to the driven shield signals[32].
4. Where possible, use 2oz copper (finished) on the PCB outer layers to improve heat flow.
5. Use a GND flood that extends on each layer up to the device pins, under the entire device body area (noting that power trace(s) will likely need to bisect the flood on one inner layer).
6. Use extra 0.3mm regular or plugged vias placed on a 1.5mm pitch to "stitch" the GND floods together electrically and thermally under the device.



7. Extend a copper GND flood from underneath the body, past the non-sensing pins (i.e. predominantly on one package edge) on the bottom layer of the PCB, to create an extra area of at least 25mm x 25mm. Keep this area wide and continuous and avoid adding narrow necks or meanders, so that the area functions as a good thermal conductor away from the device.
8. If uncertain, please contact TNx.

The above rules assume a 4-layer (minimum) PCB and that the design goal is to meet 105°C ambient temperature operation. In situations where a lower operating temperature is required (e.g. Industrial/Medical), these rules can be relaxed to a 2-layer PCB, but special care should be taken to optimize the outer layer copper floods on the rear side, to allow enough heat to flow away from the device.

[30] When soldered to PCB as described in **A.1.5 PCB Footprint Notes.**
[31] To avoid solder wicking from under the body during reflow.
[32] maximum added capacitance to the SHIELD2DCTS or SHIELDAUX nets must not be greater than 100pF.

Appendix B References

TNxAN00035 aXiom Touch Controller Comms Protocol.
TNxAN00037 aXiom Touch Controller Sensor Channel Routing.
TNxAN00043 aXiom Touch Controller Bootloader.
TNxAN00045 aXiom Touch Controller Comms Quick Start Guide.
TNxAN00048 aXiom Touch Controller EMC Report.
TNxAN00051 aXiom Driver Guide.
TNxAN00052 aXiom Project Flow.
TNxAN00056 aXiom Self Test.
TNxAN00061 aXiom Touch Controller Reduced Power Mode.
TNxD00442 Production Process with aXiom Devices.
TNxAN00047 aXiom Touch Controller Sensor Testing.
TNxAN00042 aXiom Touch Controller Sensor Compatibility.
TNxAN00038 aXiom AX112A Touch Controller Programmer's Guide.
TNxAN00044 aXiom Touch Controller AX112A EVK Quick Start Guide.

Note: Release of the above documents may require a specific NDA to be in place, please contact TouchNetix for more details.

Appendix C Legal Copyright and Disclaimer

Appendix D Document History

Revision	Date	Change summary
A1	12/06/2022	Preliminary release
A2	23/03/2023	Correction to the Absolute Maximum Ratings table for Ts and Tj values, split IO tables into 1.8V and 3.3V levels and change measurement criteria for VOH from max to min.
A3	24/03/2023	Addition of B Pin restrictions to the Pin Description table.
A4	10/08/2023	Update of a disclaimer to the reference page to highlight that before access is permitted to some documents, an NDA is required. Some referenced documents are hidden from the reference list as not currently shared in the document pack, no longer a used document or not released. Updated reference link for new Dials on display document and added to the reference list. Updated ordering information.
A5	01/10/2024	nReset capacitor value corrected to 10nF from 20nF.
A6	11/10/2024	Added Footprint information and Bootloader part number details.
A7	03/02/2025	Clarify max ABS cap loading on sense pins. Remove regions. Added information to the power sequencing section regarding the state of the I/O pins at power-up.