

1 Introduction

The aXiom AX112A-3D is an Automotive Qualified Capacitive Multi-touch controller with the very highest performance, for use in demanding applications across markets such as Automotive, Industrial, White Goods and Medical.

In addition to supporting state-of-the-art Capacitive Touch Sensing, the device also features integrated force sensing and haptic feedback output event triggers, to allow creation of rich user interfaces. Use of these features allows the device to sense not only conventional contact type touches, but also to detect the force applied to the touch sensor cover lens.

The high performance acquisition engine enables the touchscreen controller to sense regular contacts and gloves, as well as detecting pre-contact proximity and hover finger targets above the touchscreen surface. Additionally, the same sensing performance allows designers to use thick plastic front lenses, curved or non-uniform thickness lenses and even to sense through a small air gap. Industry leading water rejection and wet finger tracking is also included.

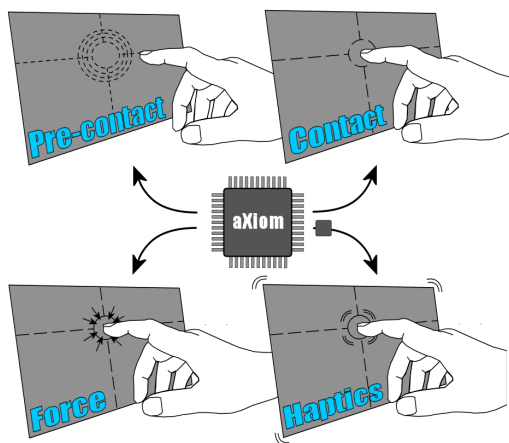


Figure 1-1: aXiom 3D Sensing Capabilities

Combined with the ability to output region based haptic feedback commands to a 3rd party driver, the device becomes the central controller for a holistic user interface system, implementing 3D proximity, 3D hover, 3D overlays/lenses, touch, force and haptic feedback.

A Windows™ based software package, TouchHub2, is provided with the AX112A-3D to ease design and tuning tasks. This allows the designer to input simplified design choices and enables TouchHub2 to automatically create optimized tuning configurations. Additionally, a digitizer driver is available for Linux.

Features at a Glance

Capacitive Multi-touch Controller

- Ultra high SNR: >80dB.
- Supports up to 112 touch sensing channels.
- Flexible channel routing allows arbitrary touch sensor aspect ratios.
- Supports non-rectangular sensors.
- Touch sensing through very thick plastic lenses and/or air gaps.
- Supports non-uniform lens thickness.
- Supports both 3D proximity and 3D hover sensing.
- Supports up to 2 Dial On Display mechanical rotors.
- All touches reported at a frame rate of up to 250Hz¹.
- Glove support without switching modes.
- Water suppression and wet finger tracking.
- Low emissions, low drive amplitude, high immunity to conducted interference.
- Host connection using SPI or I²C slave with interrupt.
- 3V3 and 1V8 supply, no high voltage generators needed.
- Independent I/O voltage supporting 1.8V to 3.3V host signaling.
- Optional external synchronization with display drivers for highest SNR.

Force Controller

- Supports up to 4 force sensing channels.
- Can detect displacement of cover lens <10um.
- Supports multi-force.
- Force measured concurrently with touch.

Haptic Trigger

- User definable region based haptics.
- Configurable hot-spot maps and actions.
- Trigger uses master I²C, SPI or GPIO output to 3rd party driver chip.

General

- Register based tuning with non-volatile configuration storage.
- Field upgradable firmware.
- Sophisticated Built-In-Self-Test routines and diagnostics.
- Automotive AEC-Q100 grade 2 qualified.
- -40°C to +105°C ambient operating temperature.
- Available in LQFP156 package.
- TouchHub2 evaluation and support software for design and tuning.

¹Subject to configuration.

2 Ordering Information

Device	Package	Part Number	Shipping
AX112A-3D LQFP156 Industrial	LQFP156 Exposed Pad 14x20x1.4mm 0.4 Pitch	838-010009	72 devices per tray
AX112A-3D LQFP156 Automotive	LQFP156 Exposed Pad 14x20x1.4mm 0.4 Pitch	838-010008	72 devices per tray

NOTE: These devices will arrive with default bootloader and firmware installed, you will then need to load your chosen firmware version once mounted on your PCB.

Contents

1 Introduction	1
2 Ordering Information	2
3 Device Pinout	6
3.1 Pin Map	6
3.1.1 LQFP156	6
3.2 Pin Table	7
3.2.1 LQFP156	7
4 Pin Descriptions	10
4.1 GND	10
4.2 A0..34, B0..2, B31..34, C0..34, D0..34	10
4.3 VDDA	10
4.4 VDDI	10
4.5 SLVnIRQ	10
4.6 SLVSDA / SCK	10
4.7 SLVSCL / nSS	10
4.8 SLVI2CADDRSEL / MOSI	11
4.9 nSLVI2C / MISO	11
4.10 MSTCOMMS0	11
4.11 MSTCOMMS1	11
4.12 MSTCOMMS2	11
4.13 MSTCOMMS3	12
4.14 GPIO0..4	12
4.15 DNC	12
4.16 nRESET	12
4.17 VDDC	12
4.18 AUX0..3	12
4.19 SHIELDAUX	12
4.20 SHIELD2DCTS	12
5 Reference Schematic	13
6 Sensing	14
6.1 Sensing Overview	14
6.2 Touch Sensing	17
6.3 Variable Thickness Lenses	20
6.4 Dial On Display	21
6.5 Force Sensing	22
6.6 Pre-contact Sensing (3D Prox and Hover)	24
6.7 EMC Features	25
6.8 Water Suppression	27
6.9 Sensor Compatibility	29
6.10 Sensor Protection	29
7 Host Interfaces	30
7.1 Available Interfaces	30
7.2 Mode Selection	30
7.3 Slave I ² C Mode	31
7.3.1 Slave Address Selection	31
7.3.2 Connections	31
7.3.3 I ² C Protocol	31
7.4 Slave SPI Mode	32
7.4.1 Device Selection	32
7.4.2 Connections	32
7.4.3 SPI Protocol	32
8 Haptics	33

9 Programming Model	34
10 Device Characteristics	35
10.1 Absolute Maximum Ratings	35
10.2 Operational Ratings	36
10.2.1 Operating Conditions	36
10.2.2 Power Requirements	36
10.2.3 Power Sequencing	36
10.2.4 Startup Time	36
10.2.5 Reduced Power Mode	37
10.2.6 CMOS I/O Characteristics	38
10.2.7 Slave I ² C Characteristics	39
10.2.8 Slave SPI Characteristics	40
10.2.9 Master I ² C Characteristics	41
10.2.10 Capacitance Ranges and Drive Limits	42
10.2.11 Non-volatile Memory Characteristics	43
10.2.12 Device BIST Capabilities	44
10.2.13 Sensor BIST Capabilities	44
10.2.14 2D CTS Diagonal Size Range Guide	45
Appendix A Package Drawings	46
A.1 LQFP156-EP14201404	46
A.1.1 Package Information	46
A.1.2 Footprint Information	47
A.1.3 Layout and Routing Considerations for VDDA tracks	48
A.1.4 Package Thermal Characteristics	50
A.1.5 PCB Footprint Notes	50
Appendix B References	51
Appendix C Legal Copyright and Disclaimer	52
Appendix D Document History	53

List of Figures

1-1 aXiom 3D Sensing Capabilities 1

3.1.1-1 LQFP156 Device Pinout (top view) 6

5-1 Reference Schematic (LQFP156) 13

6.1-1 Acquisition Engine Frame Structure 15

6.1-2 Simplified System Architecture 16

6.1-3 Simplified Sensing Architecture 16

6.2-1 Channel Naming Convention 17

6.2-2 Traditional vs. aXiom Channel Allocation 19

6.3-1 Example of a Flat Sensor and Variable Thickness Lens 20

6.5-1 Single-Force System Implementation, Non-segmented CDS 22

6.5-2 Multi-Force System with Four Force Channels, Quadrant-segmented CDS 23

6.6-1 Sensing a Target Before Contact With The CTS 24

6.7-1 Example Common Mode Noise From “Other” Equipment 25

6.8-1 Different Behaviors With Abs-cap and Trans-cap Measurements With Water and Touch 27

7.2-1 Communication Mode Selection 30

7.3.2-1 Slave I²C Connections 31

7.4.2-1 Slave SPI Connections 32

8-1 Master I²C Connections to 3rd Party Device(s) 33

10.2.7-1 Typical I²C Transaction and Parameters 39

10.2.8-1 Typical SPI Transaction and Parameters 40

10.2.14-1 2D CTS Diagonal Size Range Guide 45

A.1.1-1 Package Drawing 46

A.1.2-1 Footprint Drawing 47

A.1.3-1 C-shaped power routing, balanced amongst all VDDA pins. Figure shows an AX198A, same advice can be applied to this device. 49

A.1.3-2 Note the use of the widest possible tracking and multiple vias for all VDD tracks. Figure shows an AX198A, same advice can be applied to this device. 49

List of Tables

3.2.1-1 LQFP156 Pin Table 9

3.2.1-2 Pin Classes 9

7.3.1-1 Slave I²C Address Selection 31

10.1-1 Absolute Maximum Ratings 35

10.2.1-1 Operating Conditions 36

10.2.2-1 Power Requirements 36

10.2.6-1 CMOS I/O Characteristics (1.8V) 38

10.2.6-2 CMOS I/O Characteristics (3.3V) 38

10.2.7-1 Timings 39

10.2.8-1 Timings 40

10.2.10-1 Capacitance Ranges and Drive Limits 42

10.2.10-2 REFCAP Requirements 42

10.2.11-1 Non-volatile Memory Characteristics 43

3 Device Pinout

3.1 Pin Map

3.1.1 LQFP156

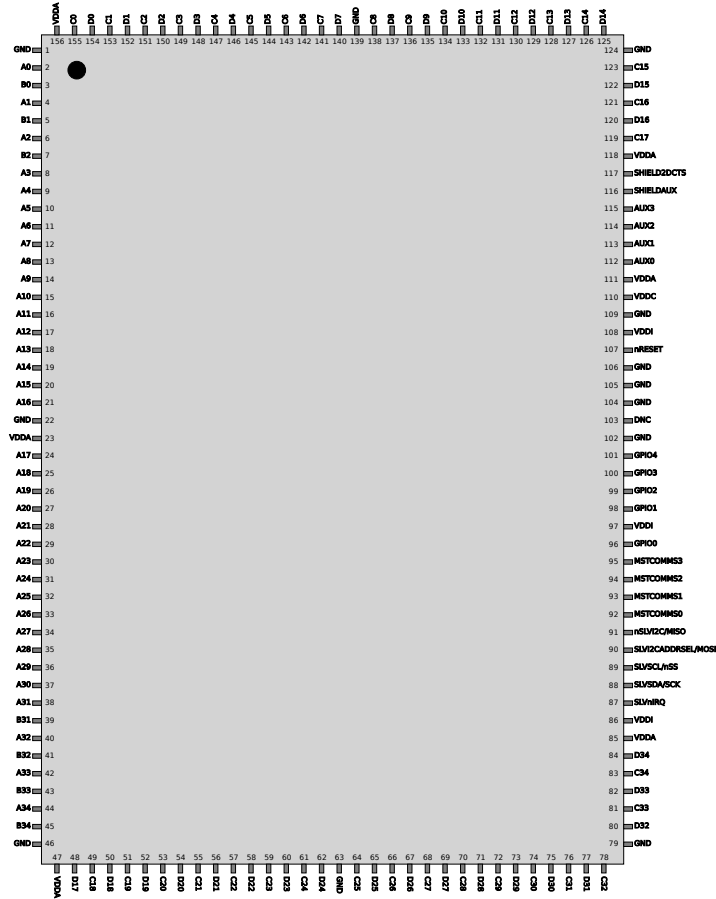


Figure 3.1.1-1: LQFP156 Device Pinout (top view)

3.2 Pin Table

3.2.1 LQFP156

Pin Number	Name	Class	Domain	Function	If not required	Notes
1	GND	PWR		Supply and signal reference	Not applicable	
2	A0	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
3	B0	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
4	A1	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
5	B1	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
6	A2	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
7	B2	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
8	A3	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
9	A4	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
10	A5	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
11	A6	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
12	A7	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
13	A8	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
14	A9	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
15	A10	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
16	A11	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
17	A12	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
18	A13	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
19	A14	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
20	A15	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
21	A16	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
22	GND	PWR		Supply and signal reference	Not applicable	
23	VDDA	PWR		Analogue supply	Not applicable	
24	A17	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
25	A18	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
26	A19	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
27	A20	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
28	A21	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
29	A22	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
30	A23	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
31	A24	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
32	A25	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
33	A26	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
34	A27	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
35	A28	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
36	A29	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
37	A30	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
38	A31	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
39	B31	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
40	A32	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
41	B32	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
42	A33	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
43	B33	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
44	A34	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
45	B34	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
46	GND	PWR		Supply and signal reference	Not applicable	
47	VDDA	PWR		Analogue supply	Not applicable	
48	D17	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
49	C18	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
50	D18	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
51	C19	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
52	D19	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
53	C20	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
54	D20	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
55	C21	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
56	D21	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
57	C22	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
58	D22	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
59	C23	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
60	D23	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
61	C24	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
62	D24	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
63	GND	PWR		Supply and signal reference	Not applicable	
64	C25	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
65	D25	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	

Pin Number	Name	Class	Domain	Function	If not required	Notes
66	C26	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
67	D26	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
68	C27	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
69	D27	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
70	C28	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
71	D28	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
72	C29	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
73	D29	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
74	C30	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
75	D30	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
76	C31	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
77	D31	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
78	C32	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
79	GND	PWR		Supply and signal reference	Not applicable	
80	D32	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
81	C33	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
82	D33	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
83	C34	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
84	D34	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
85	VDDA	PWR		Analogue supply	Not applicable	
86	VDDI	PWR		I/O supply	Not applicable	
87	SLVnIRQ	OD	VDDI	Slave report ready interrupt	Leave no connect	Requires additional pull up if used.
88	SLVSDA / SCK	ODwpu (may change to lwpu during startup)	VDDI	Slave I ² C data OR SPI SCK	Not applicable	Requires additional pull up if using I ² C mode.
89	SLVSL / nSS	ODwpu (may change to lwpu during startup)	VDDI	Slave I ² C clock OR SPI nSS	Not applicable	Requires additional pull up if using I ² C mode.
90	SLV2CADDRSEL / MOSI	lwpu	VDDI	Slave I ² C address select OR SPI MOSI	Not applicable	In I ² C mode, controls address. In SPI mode becomes MOSI input from host.
91	nSLV2C / MISO	lwpu (may change to O during startup)	VDDI	Slave I ² C mode OR SPI MISO	Not applicable	Sampled at reset; if low selects I ² C mode, if high selects SPI mode and becomes MISO output to host.
92	MSTCOMMS0	O / I / ODwpu	VDDI	Master Comms port	Leave no connect	
93	MSTCOMMS1	O / I / ODwpu	VDDI	Master Comms port	Leave no connect	
94	MSTCOMMS2	O / I / ODwpu	VDDI	Master Comms port	Leave no connect	
95	MSTCOMMS3	O / I	VDDI	Master Comms port	Leave no connect	
96	GPIO0	IOwpu	VDDI	General purpose I/O	Leave no connect	
97	VDDI	PWR		I/O supply	Not applicable	
98	GPIO1	IOwpu	VDDI	General purpose I/O	Leave no connect	Optionally serves as HSYNC input.
99	GPIO2	IOwpu	VDDI	General purpose I/O	Leave no connect	Optionally serves as VSYNC/EXTSYNC input.
100	GPIO3	IOwpu	VDDI	General purpose I/O	Leave no connect	
101	GPIO4	IOwpu	VDDI	General purpose I/O	Leave no connect	
102	GND	PWR		Supply and signal reference	Not applicable	
103	DNC			Do not connect		
104	GND	PWR		Supply and signal reference	Not applicable	
105	GND	PWR		Supply and signal reference	Not applicable	
106	GND	PWR		Supply and signal reference	Not applicable	
107	nRESET	lwpu	VDDI	Hardware reset	Not applicable	May require additional bypass capacitor to GND for best EMC.
108	VDDI	PWR		I/O supply	Not applicable	
109	GND	PWR		Supply and signal reference	Not applicable	
110	VDDC	PWR		Core supply		Output from internal LDO.
111	VDDA	PWR		Analogue supply	Not applicable	
112	AUX0	AIO	VDDA	Auxiliary sense pin	Leave no connect	Sense pin for force sensing.
113	AUX1	AIO	VDDA	Auxiliary sense pin	Leave no connect	Sense pin for force sensing.
114	AUX2	AIO	VDDA	Auxiliary sense pin	Leave no connect	Sense pin for force sensing.
115	AUX3	AIO	VDDA	Auxiliary sense pin	Leave no connect	Sense pin for force sensing.
116	SHIELDAUX	AO	VDDA	Auxiliary shield pin	Leave no connect	Shield driver for AUX sense pins.
117	SHIELD2DCTS	AO	VDDA	2DCTS shield pin	Not applicable	Shield driver for 2DCTS sense pins.
118	VDDA	PWR		Analogue supply	Not applicable	
119	C17	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
120	D16	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
121	C16	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
122	D15	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
123	C15	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
124	GND	PWR		Supply and signal reference	Not applicable	
125	D14	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
126	C14	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
127	D13	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
128	C13	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
129	D12	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
130	C12	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	

Pin Number	Name	Class	Domain	Function	If not required	Notes
131	D11	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
132	C11	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
133	D10	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
134	C10	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
135	D9	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
136	C9	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
137	D8	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
138	C8	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
139	GND	PWR		Supply and signal reference	Not applicable	
140	D7	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
141	C7	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
142	D6	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
143	C6	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
144	D5	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
145	C5	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
146	D4	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
147	C4	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
148	D3	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
149	C3	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
150	D2	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
151	C2	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
152	D1	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
153	C1	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
154	D0	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
155	C0	AIO	VDDA	Sense pin	Connect to SHIELD2DCTS	
156	VDDA	PWR		Analogue supply	Not applicable	

Table 3.2.1-1: LQFP156 Pin Table

Class	Description
PWR	Power pin
AI	Analogue input
AO	Analogue output
AIO	Analogue IO
I	CMOS input (no pull up)
Iwpu	CMOS input with weak pull up ²
O	CMOS push-pull output
ODwpu	CMOS Open drain with weak pull up ²
OS	CMOS Open source no pull down
OD	CMOS Open drain no pull up
IO	CMOS input/output
IOwpu	CMOS input/output with weak pull up ²

Table 3.2.1-2: Pin Classes

As a general convention, communication pin names are prefixed with "SLV" or "MST" to designate Slave or Master. Pin names with an "n" at the start of the function name designate an active-low signal e.g. MSTnIRQ is an active low interrupt from the Master. Also note that dual-mode pins are named (A) / (B), where (A) is the applicable name in the first mode and (B) in the second mode.

²Pull up/down intended as level keeper only.

4 Pin Descriptions

4.1 GND

The 0V power supply connection. Connect all GND pins to 0V.

4.2 A0..34, B0..2, B31..34, C0..34, D0..34

4.3 VDDA

The analogue sub-system's power supply connection, running at nominally 3.3V. Connect all VDDA pins to 3.3V. The VDDA supply must be low noise and well regulated. Each VDDA pin must have a parallel 22uF and 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. An additional single bulk ceramic, tantalum or electrolytic capacitor of $\geq 22\mu\text{F}$ is required on the VDDA supply. Under most conditions its is acceptable to share this supply with VDDI³.

These pins have special layout considerations. See **Appendix A.1.3 Layout and Routing Considerations for VDDA tracks** for further details.

4.4 VDDI

The I/O sub-system's power supply connection, running at nominally 1.8V to 3.3V. Connect all VDDI pins to this supply. The VDDI supply is used to define the interface logic level used to communicate with the host, so must be sufficiently well regulated to ensure reliable high speed comms. Each VDDI pin must have a 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. If the VDDA and VDDI supplies are separate, an additional single bulk ceramic, tantalum or electrolytic capacitor of $\geq 1\mu\text{F}$ is required on the VDDI supply. Under most conditions it is OK to share this supply with VDDA, in which case route VDDI as a separate net and use a star point connection to VDDA to help to isolate noise on the two domains³. CMOS I/O pins should never exceed the limitations stated in Table 10.1-1 (V_{pc} and V_{pa}) during power up, operation or power down.

These pins have special layout considerations. See **Appendix A.1.3 Layout and Routing Considerations for VDDA tracks** for further details.

4.5 SLVnIRQ

The device generates an interrupt whenever it has a report waiting to be read by the host. The slave interrupt pin asserts low in this case. It returns to a Hi-Z state when no reports are pending (but is weakly pulled up). The action of the host reading a report is to consume that report, and when all reports have been consumed the pin returns to Hi-Z (wpu). In order to affect an acceptably fast low-to-high transition in the presence of parasitic capacitance, an external pull up of 1K to 10K is required. The host device should use *level* triggering to sense the interrupt.

4.6 SLVSDA / SCK

This pin serves different functions depending on the communication mode selected by the nSLVI2C pin:

Slave I²C Mode: The pin serves as the I²C Data pin to connect to the host. It has a weak internal pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.

Slave SPI Mode: This pin becomes the SPI SCK clock input from the host. In this mode no additional pull-up resistor is required.

4.7 SLVSCL / nSS

This pin serves different functions depending on the communication mode selected by the nSLVI2C pin:

Slave I²C Mode: This pin is the I²C Clock pin to connect to the host. It has a weak internal pull

³Assuming the I/O level is 3.3V.

up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.

Slave SPI Mode: This pin becomes the SPI active low Slave Select input from the host. In this mode no additional pull-up resistor is required.

4.8 SLVI2CADDRSEL / MOSI

This pin serves different functions depending on the communication mode selected by the nSLVI2C pin:

Slave I²C Mode: Selects between 2 addresses for the device. See **7.3.1 Slave Address Selection** for details. The pin includes a weak pull up. It is strongly recommended to terminate this pin directly to GND or VDDI (as required) to completely override this pull up (but only when in Slave I²C mode!).

Slave SPI Mode: The pin becomes the MOSI input from the host.

4.9 nSLVI2C / MISO

This pin serves different functions depending on its state as sampled at power-on or reset:

Sampled low at reset: Selects Slave I²C communications mode. The pin includes a weak pull up. It is strongly recommended to terminate this pin directly to GND to select Slave I²C mode.

Sampled high at reset: Selects Slave SPI communications mode. The pin includes a weak pull up. It is strongly recommended to use a supplemental pull-up of 1K to 10K to select SPI mode; the pin must not be terminated directly to VDDI ! On switching to SPI mode, the pin is changed to an output driver and is used as the MISO output to the host.

4.10 MSTCOMMS0

The device has a Master Communications port which can be controlled by a renderer in one of 3 modes: as a GPIO parallel output, as a master I²C interface or as a master SPI interface.

GPIO mode: this is the first output driver OUTA.

I²C mode: this is the Master I²C Data pin MSTSDA. It has a weak internal pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.

SPI mode: this is the MOSI output data pin MSTMOSI to the slave.

4.11 MSTCOMMS1

The device has a Master Communications port which can be controlled by a renderer in one of 3 modes: as a GPIO parallel output, as a master I²C interface or as a master SPI interface.

GPIO mode: this is the second output driver OUTB.

I²C mode: this is the Master I²C Clock pin MSTSCL. It has a weak internal pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.

SPI mode: this is the SCK clock output pin MSTSCK to the slave.

4.12 MSTCOMMS2

The device has a Master Communications port which can be controlled by a renderer in one of 3 modes: as a GPIO parallel output, as a master I²C interface or as a master SPI interface.

GPIO mode: this is the third output driver OUTC.

I²C mode: this is the active low interrupt pin MSTnIRQ. It has a weak internal pull up which may need to be supplemented depending on the nature of the driver connected to it. If the interrupt is shared between 2 or more devices, then each must be capable of indicating via I²C commands whether it is actively asserting its interrupt or not.

SPI mode: this is the MISO input data pin MSTMISO from the slave.

4.13 MSTCOMMS3

The device has a Master Communications port which can be controlled by a renderer in one of 3 modes: as a GPIO parallel output, as a master I²C interface or as a master SPI interface.

GPIO mode: this is the forth output driver OUTD.

I²C mode: not used

SPI mode: this is the nSS active low slave select output pin MSTnSS to the slave.

4.14 GPIO0..4

General purpose I/O pins that can be configured and used by the host as required. Each one has an internal weak pull up included. Note the optional use of GPIO1 as an HSYNC input and GPIO2 as a VSYNC/EXTSYNC input (these optional selections are made via the device's configuration registers).

4.15 DNC

Do not connect. This pin has an internal connection to the device and must not be connected externally.

4.16 nRESET

This pin is the asynchronus master hardware reset. Asserted low it returns the device to its reset state. When high, the device operates as normal. The pin has a weak internal pull up which must be supplemented with a 1K to 5K pull up and optionally a 10nF ceramic bypass capacitor to GND⁴ (to offer the best fast-transient immunity in harsh EMI applications).

4.17 VDDC

The core sub-system's power supply output, driven by an internal LDO running at nominally 1.8V. If there is more than one VDDC pin then connect them all together to form a single net. Each VDDC pin must have a parallel 22uF and 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. No other connections to the VDDC net are permitted.

These pins have special layout considerations. See **Appendix A.1.3 Layout and Routing Considerations for VDDA tracks** for further details.

4.18 AUX0..3

The auxiliary channels are used for force sensing. A single channel force system uses AUX0 only. A multi-channel force system uses all four channels. The routing and layout of the connections to these pins is critical and is described in a separate application note. See **Appendix B References**. AUX3 can also be used (in single channel mode) to measure a reference capacitor to facilitate factory test and avoid the need for per-unit calibration.

4.19 SHIELDAUX

The auxiliary sense pins must be routed using a shielding technique using a dummy electrode that is driven by this pin. This is described in a separate application note. See **Appendix B References**.

4.20 SHIELD2DCTS

The 2D CTS sense pins must be routed using a shielding technique using a dummy electrode that is driven by this pin. This is described in a separate application note. See **Appendix B References**. SHIELD2DCTS must be bypassed to GND near to the device, with a single 1nF 6V ceramic X5R (or tighter tolerance) capacitor.

⁴Check the ability of the connected reset driver to support this capacitive load.

6 Sensing

6.1 Sensing Overview

The aXiom sensing architecture has been designed to measure capacitance, with a Signal-To-Noise ratio that goes far beyond existing solutions, whilst also being sympathetic to the diverse range of EMC and EMI challenges that are faced in real-world applications. Using a high purity narrow band drive waveform, with an amplitude of just 1.25V⁵, the controller not only has extremely low Radiated Emissions but is also sympathetic to the long term sensor ageing problem, that is seen when operating at elevated temperature and humidity. This little-documented aspect of touch sensors, can only be addressed by using low amplitude DC-neutral drive techniques, to radically slow down the effects of electro-corrosion, electro-migration and e-field induced damage to various metals and some polymeric materials. To pass stringent EMC tests, in particular those dealing with injected currents (Conducted Immunity), many competing controllers resort to high sensor drive amplitudes to improve their overall SNR. While this may be successful in one regard, it seriously compromises both sensor lifetime and Radiated Emissions. Coupled with drive waveforms that are often square in nature (leading to complex harmonic content), it can be seen that a pure low amplitude drive signal is a major advantage in tough environments. To measure capacitance using small signals in the presence of large amounts of external noise, requires that the sensing architecture and the analogue front end of the device, is carefully optimized to be able to recover the carrier, even when this is hundreds of times smaller than the interference; techniques that are well understood in modern radio systems but that are seldom used in touch sensing.

The device can be connected to a broad range of Capacitive Touch Sensor (CTS) styles, including both single and double connected versions of the well known *Diamond*, *Flooded* and *True Single Layer* types. To further extend the range of applications that are possible, the device treats its sensor pins as general resources and is able to use any pin as either drive or sense. This allows great flexibility in the aspect ratio of the CTS sensing area; the pool of sensor pins can be mapped to sensor electrodes in any ratio that is needed. This allows everything from long-thin touch areas to square touch areas to be created easily. The sensing architecture has more than enough dynamic range to handle the sensor measurement, in the presence of the diverse parasitics created by such extreme aspect ratios. This capability further extends to allowing direct support for truncated electrodes, often found in non-rectangular touch applications⁶.

The high SNR of the acquisition engine, allows a wide range of glove types and thicknesses to be used with the CTS. Alternatively, high quality multi-touch tracking through very thick plastic cover panels becomes possible; over 10mm of acrylic overlay can be used and can even have varying thickness, thanks to a novel compensation scheme that helps to unify the touch sensitivity across diverse thickness changes. Sensing through small air gaps also becomes viable⁷. Water suppression is built into the device's capability, allowing wet finger tracking and water rejection⁸.

⁵2.5V pk-pk

⁶Imagine a circular sensor; the outer electrodes have almost no surface area compared to those in the middle.

⁷Subject to mechanical stability considerations.

⁸Including saline solutions, blood etc with some sensing compromises.

The acquisition engine makes its measurements during a period called a Frame. Each frame is subdivided into smaller time units called *Slots*. During a Frame, different measurement tasks (Slots) are scheduled. Typically, a Frame consists mainly of CTS and/or CDS Slots, simply because there are so many measurements to take. There are also typically, a small number of Slots used for housekeeping. To simplify things, TouchHub2 can automatically configure the Frame based on the system's requirements.

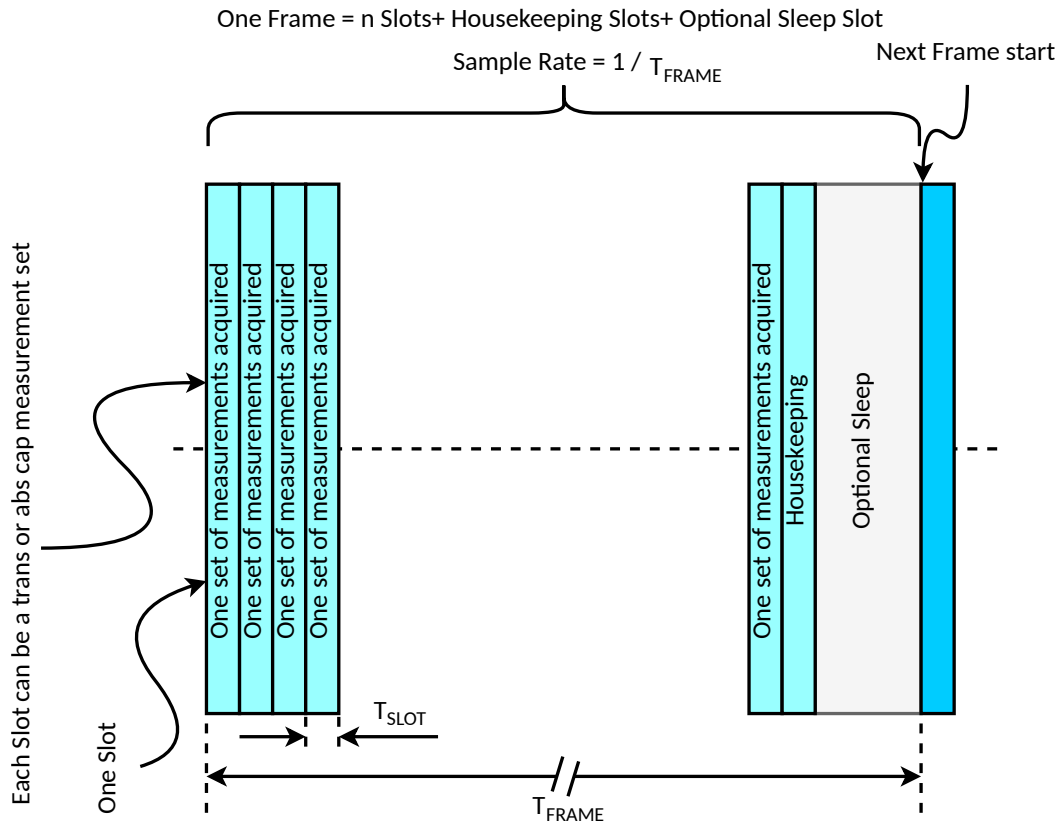


Figure 6.1-1: Acquisition Engine Frame Structure

The overall architecture of the AX112A-3D is shown below in simplified form.

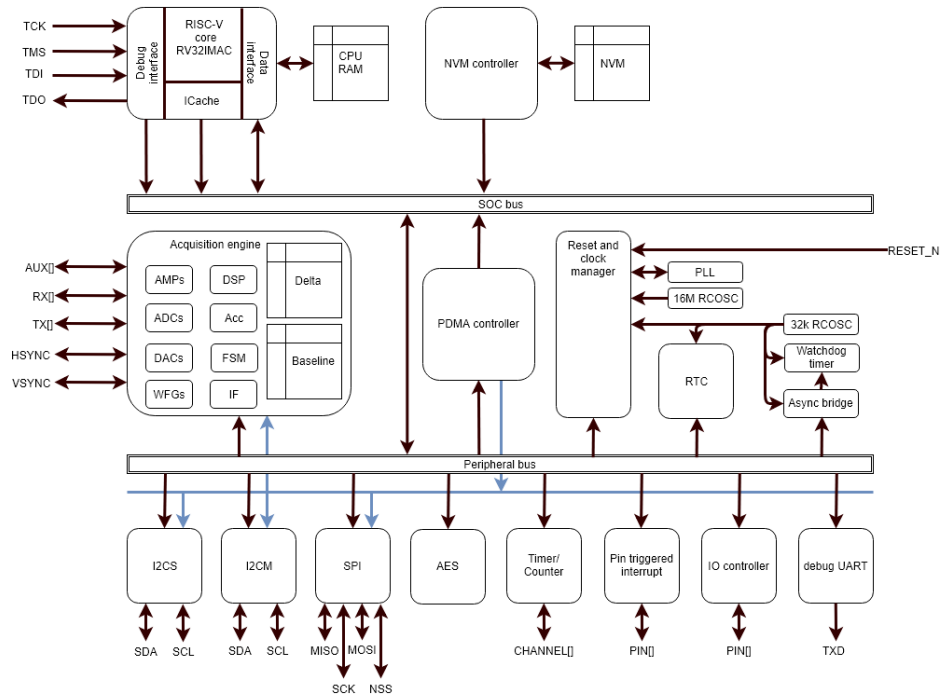


Figure 6.1-2: Simplified System Architecture

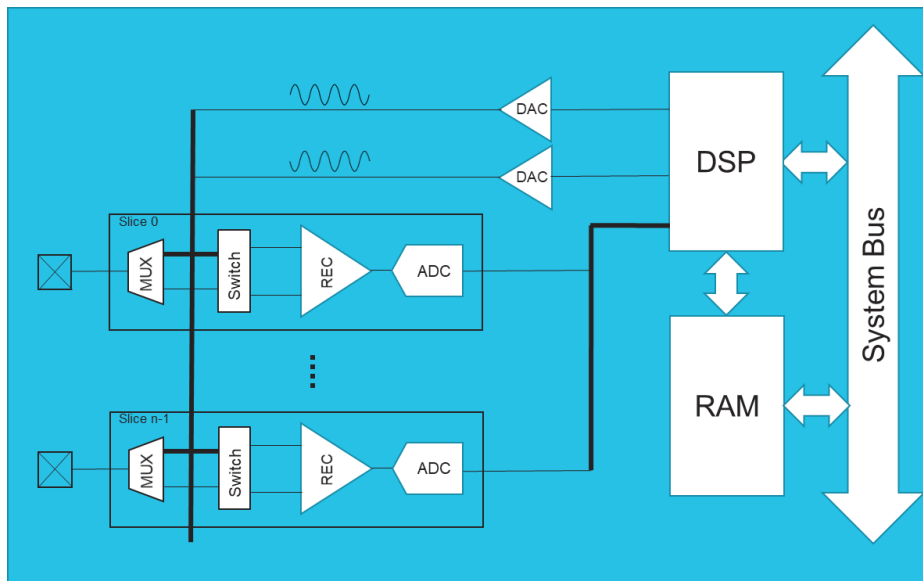


Figure 6.1-3: Simplified Sensing Architecture

6.2 Touch Sensing

The AX112A-3D uses a *transverse capacitive* measurement technique (“trans-cap”) to sense the capacitive coupling between pairs of electrodes. Traditionally, these would be called *transmitter* and *receiver* (or *drive* and *sense*) electrodes. The AX112A-3D sensing architecture is more flexible than existing devices, which makes it misleading to think of electrodes as having fixed transmit and receive functions. Rather, any electrode can be either function. Hence, we’ll refer to them as either just electrodes or *sense pins* or even sometimes *channels*; the names are freely interchangeable.

The AX112A-3D has 112 sense pins. These can be wired to the electrodes of a 2D Capacitive Touch Sensor (2D CTS) in a very flexible way, enabling the creation of sensing areas with arbitrary aspect ratios. To simplify the design task, the supplied TouchHub2 software can take high-level design requirements, such as the number of electrodes in each axis of the CTS, and automatically decide which device pins to connect to which electrodes. For this reason, when you look in the Pin Description tables you will not see familiar names like “TX0” or “RX10”. Instead, you will see pins with more generic names like “A0” and “D3”. This way we reduce the risk of inferring the function of these pins. Likewise, we refer to the two axes as Rows and Columns rather than Tx and Rx.

The 2D CTS is typically formed of a grid of orthogonal electrodes. Where a Row and Column electrode intersect, a sensing node is formed. The capacitance of all nodes in the CTS are measured by the device once every *frame*⁹. When a user touches the CTS, the node capacitances change near to the touch position and cause what is referred to as a *touch delta*. It is this touch delta that the device senses and converts into accurate touch positions.

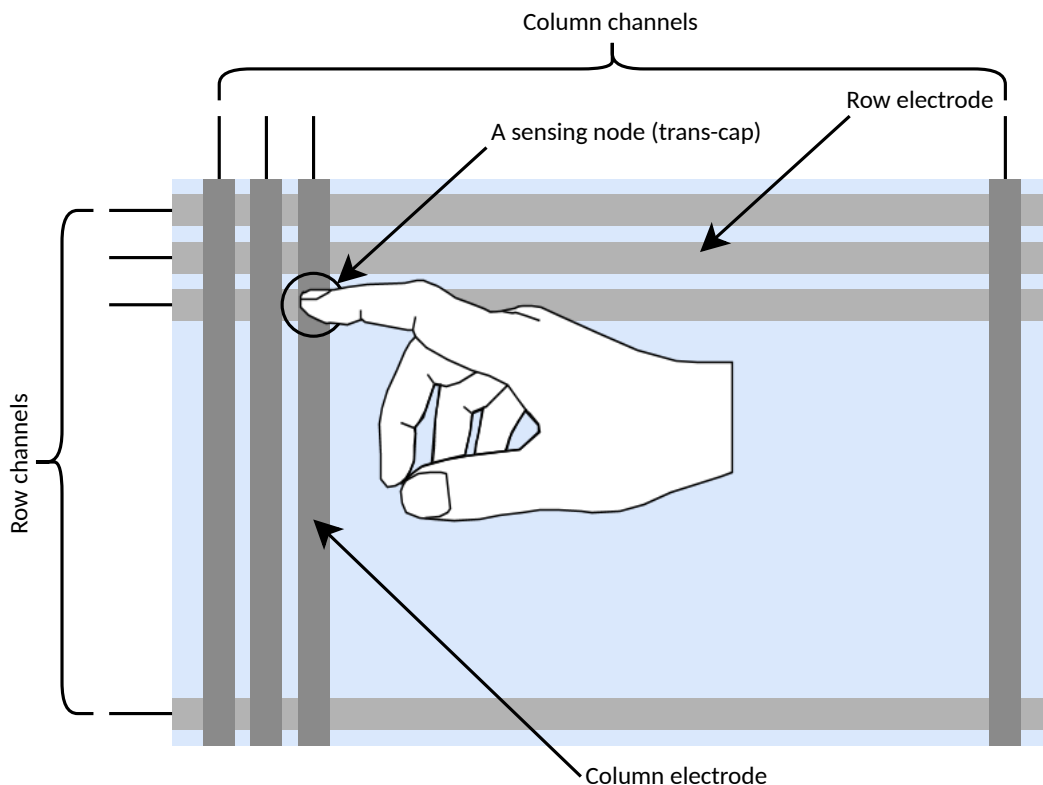


Figure 6.2-1: Channel Naming Convention

⁹The measurement is conducted by the acquisition engine, which is instructed what to do by a configuration *profile* created by TouchHub2.

The AX112A-3D can measure up to 3136 nodes; this means that configurations where $(RXs \times TXs \leq 3136)$ are supported. Some large, almost square, designs may need to limit the number of RX and TX to stay within this limit. While any pin can be configured as either TX or RX, there are multiple factors which affect performance including how electrodes are assigned to pins. Therefore, it is necessary to use the TouchHub2 tool to determine the optimal connections to use for your sensor.

The AX112A-3D can report up to 10 concurrent touches, using advanced signal processing techniques to accurately resolve touch positions at up to 16 bits of resolution. To enhance the rate at which the host can read the status and position of these touches, all 10 touches are combined into a single compact report, reducing communication traffic and reducing the chance of the host missing important touch events.

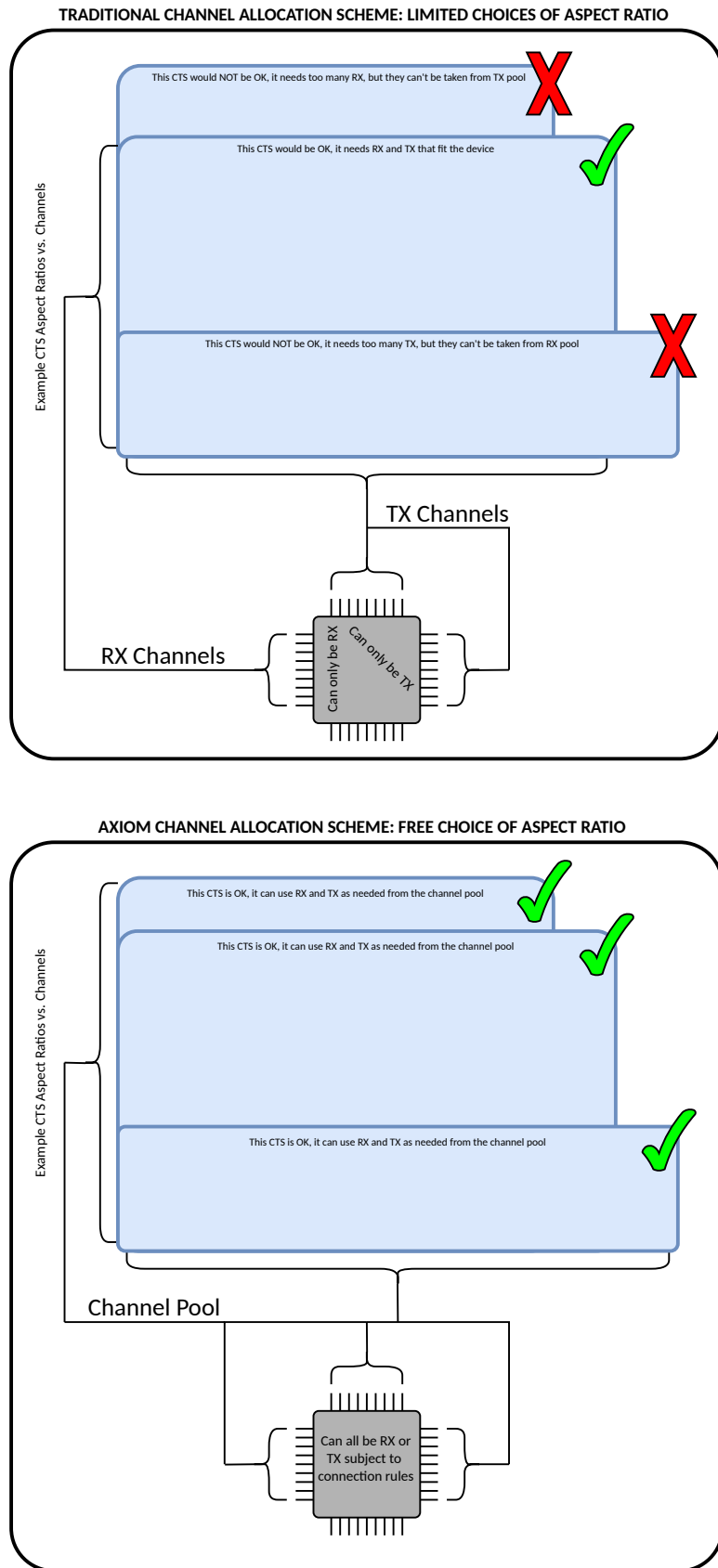


Figure 6.2-2: Traditional vs. aXiom Channel Allocation

6.3 Variable Thickness Lenses

The AX112A-3D's acquisition engine includes a facility to scale the measured 2D touch delta array on a node-by-node basis. The scaling factors for each node can be changed using TouchHub2 via a configuration file. For most touch controllers, scaling the measured deltas in this way would simply amplify the background noise, to a point where it would cause excessive touch position jitter and even false detections. However, because the SNR of the AX112A-3D is so much higher, this amplification becomes viable, allowing corrections to the apparent gain of each and every node on the 2DCTS.

This delta scaling opens up interesting new possibilities to support cover lenses with widely varying thicknesses across their surface. The scaling allows both attenuation and amplification, giving an adjustment range of x16 between areas requiring the lowest and highest gains. Additionally, any node can be completely suppressed, allowing regions of the sensor to be disabled. The rear side of the lens can remain flat, or perhaps curved in just 1 direction, making production lamination far easier than some schemes, that try to in-mould laminate the touch sensor into complex uniform thickness lenses.



Figure 6.3-1: Example of a Flat Sensor and Variable Thickness Lens

6.4 Dial On Display

The AX112A-3D supports up to four Dial On Display mechanical rotors. This is achieved by using the existing 2DCTS touch electrodes. The AX112A-3D can be configured to detect when the dial is actively being touched. To provide user feedback, the AX112A-3D can trigger haptic effects both when the dial is pressed and during its rotation. It employs the same reporting mechanism as regular touches, simplifying host support and integration.

For further details see **TNxAN00079 aXiom Dial on Display**.

6.5 Force Sensing

The AX112A-3D has 4 AUX abs-cap channels, suitable for measuring the Capacitive Displacement Sensor (CDS) used in force sensing systems. This style of sensor offers very high mechanical dynamic range, making it suitable for use in systems where alignment and stack tolerance would saturate other types of sensor. In order to harness this wide operating range, yet still measure the CDS with sufficient resolution¹⁰, the AX112A-3D uses up to 4 channels that are able to reduce the measurement burden caused by the large baseline capacitance of the CDS. Combined with the high SNR of the acquisition engine, force sensing systems can be designed that are virtually immune to wide manufacturing tolerances, yet can resolve displacements of microns.

Many force sensing systems require only a single channel to detect the overall displacement of a cover lens, relative to the system's chassis. This is a so-called *single-force* system and is suitable for most applications; each touch contact is assigned the same force and hence, is suitable for User Interfaces where the predominant mode of operation is *single touch with force qualification*; multiple touch gestures are still supported but do not need any force element to function. On the other hand, using 4 channels allows the creation of a force sensing system that can approximate the force independently on 2 touches; a *multi-force* system. Mechanically, the setup is identical to a single-force system but the CDS is split into 4 quadrants, and each part is measured by one of the 4 AUX channels. When operating in this mode, the AX112A-3D can report an approximate force coordinate i.e. the XY location where the Centre of Mass (CoM) is calculated to be¹¹.

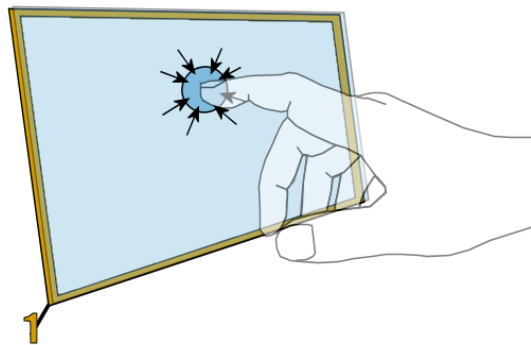


Figure 6.5-1: Single-Force System Implementation, Non-segmented CDS

¹⁰Resolve displacements of just a few micro-meters.

¹¹Channel matching becomes more critical in this case and requires more attention to tolerances and offsets.

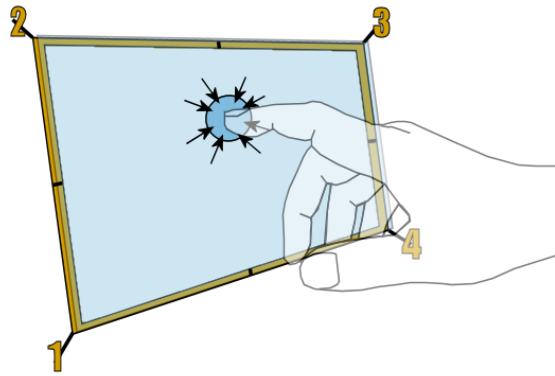


Figure 6.5-2: Multi-Force System with Four Force Channels, Quadrant-segmented CDS

The acquisition engine can be programmed to measure the CDS in the same frame as it is performing its trans-cap measurements on the 2DCTS. Hence the measurement frame rate is identical to that of the touch system and time correlation of the 2 types of measurement is guaranteed by design.

The aXiom force sensing system uses a patented CDS that has a very wide mechanical operating range and hence can absorb large assembly tolerance variation between production units, whilst maintaining excellent force sensitivity.

To ease production testing of systems equipped with force sensing, AUX 3 can have an accurate reference capacitor connected between it and GND; this is instead of a normal AUX sense channel. This allows precise and absolute measurement of the CDS's capacitance at run-time. This facility can be used as part of a design-time characterization of the mechanical displacement vs. the CDS's capacitance. Using this reference table, the AX112A-3D can be used to estimate the mechanical gap of any assembled unit, to allow a production time check that it is within tolerance. It is important to stress that having such a wide operating window, coupled with the ability to check any unit's assembly tolerance, means that *there is no need to individually reference each unit during production*.

For further information on force sensing applications, see **TNxAN00085 aXiom Force Sensing**.

6.6 Pre-contact Sensing (3D Prox and Hover)

In order to sense a target before it makes physical contact with a capacitive touch sensor, it requires the ability to sense extremely small changes in capacitance. A *normal* contact target (a touch) will typically cause a change in trans-capacitance of 10's to 100's of Femto Farads ($1\text{fF} = 10^{-15}\text{F}$). A *pre-contact* target, on the other hand, will cause a change in capacitance that is closer to 100's of Atto Farads ($1\text{aF} = 10^{-18}\text{F}$). Clearly, high measurement SNR is key to being able to detect such targets.

Competing pre-contact solutions use extra sensing electrodes positioned around the outside edge of the 2DCTS. While this allows good detection range while hovering over, or close to the electrodes, the zone in the middle of the 2DCTS is far enough away to suffer a large drop in signal, making the centre zone less sensitive¹². The 2DCTS itself also acts as a heavy load on the extra electrodes, causing substantial parasitic capacitance on them, making the measurement system work even harder to detect small changes.

In contrast, the AX112A-3D can sense and report an approximate XY position for a pre-contact target without the use of additional electrodes. It can do this because it can achieve a hardware measurement SNR of over 80dB, or 1 part in 10000. When combined with firmware DSP techniques, it can sense a pre-contact target **above the 2DCTS** at a distance of over 100mm ("Prox") and start to resolve its XY position at over 50mm ("Hover"). This is achieved without needing extra sense electrodes, and hence no extra edge margin is consumed around the outside edge of the touch panel.

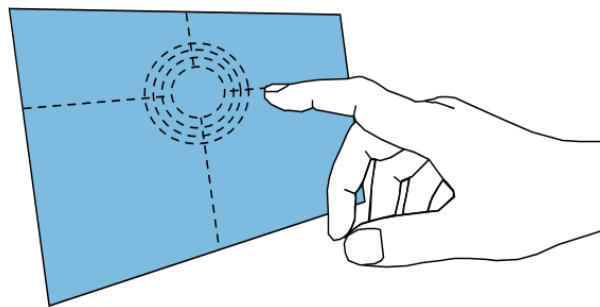


Figure 6.6-1: Sensing a Target Before Contact With The CTS

To further simplify the use of this feature, pre-contact targets are reported in exactly the same way as contact targets, but they have a flag to identify them as pre-contact together with a confidence factor, to give an indication of how far away (or weak) the pre-contact target is. This allows the host to qualify the use of the XY coordinates and take appropriate action based on the certainty of the report. Once a target makes contact with the 2DCTS, the AX112A-3D automatically reverts to a conventional touch mode, tags each detected target as a contact type and replaces the confidence factor with the force value detected from the CDS (if used)¹³.

¹²Exactly the zone that requires the greatest sensitivity.

¹³The system can detect and report a single pre-contact target, or multiple contact targets but not both at the same time.

6.7 EMC Features

One of the toughest challenges faced by capacitive touch sensors, is that of achieving high electrical noise immunity to conducted interference. The reason is simple: in most typical electronic systems we only need to worry about noise on the power supplies relative to our own GND (0V), which is local to the system. Excess noise can always be filtered out. In a capacitive touch system, part of the sensing current travels via a capacitively coupled route, through the touching finger and back to the controller *via a 3rd terminal; earth*. So noise that is *common* to power *and* GND relative to earth, will appear in the capacitive measurement when, and only when, a touch is applied. In some compliance tests, this immunity aspect is checked by injecting a *common mode* signal and sweeping it from 150KHz to 80MHz, 80% amplitude modulated. This causes a voltage disturbance of nearly 50V peak-to-peak with respect to earth¹⁴! Noise of this type is encountered in many industrial, medical and automotive environments, caused by switch mode power supplies, inductive coupling between equipment cables etc. Clearly, because the noise is “earth referred” there is no obvious conventional way to filter it.

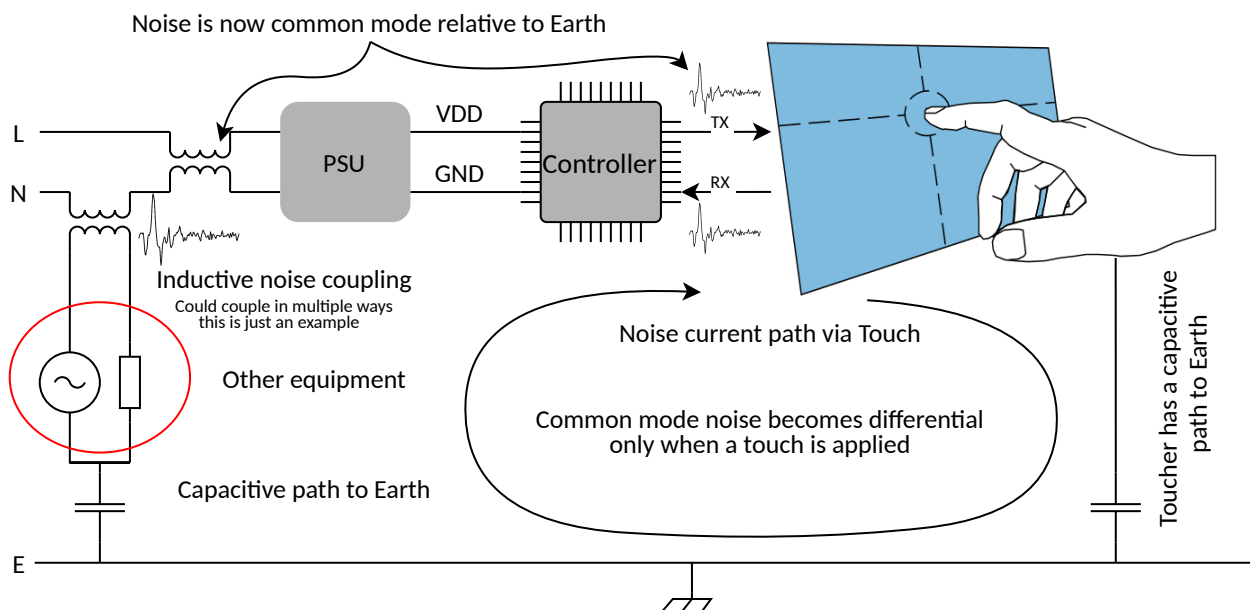


Figure 6.7-1: Example Common Mode Noise From “Other” Equipment

The nature¹⁵ of a typical touch sensor is that capacitance measurements at a frequency between 50 and 500KHz tend to be optimal. Clearly this frequency range overlaps the test band mentioned above; injecting noise at or near the measurement frequency will directly affect the measurement. In order to counter this, the AX112A-3D is frequency agile, being able to move its measurement frequency at will. This is known as *frequency hopping* and is a well understood method for avoiding interference in many aspects of electronics and radio communications¹⁶. The AX112A-3D uses a very narrow bandwidth to measure capacitance. This has the great advantage that in a congested spectrum with narrow *quiet gaps*, it is still possible to relocate the acquisition frequency to affect low noise measurements. Many competing touch devices use an *integration* technique, employing an integrator with a sampled input. This gives rise to an extremely wide and complex *reception spectrum*¹⁷, making it hard to hop away from interference. A second advantage that narrow band demodulation offers, is that it is possible to very accurately measure the amount of external noise present at any moment; the AX112A-3D does this continuously each frame and hence it can react instantly if noise suddenly appears in the system. Competing systems can sometimes be fooled into thinking that there is zero noise, when certain noise frequencies are injected, and hence their measurements fail when no preventative steps are taken to frequency hop. The AX112A-3D can never be fooled in this way. The AX112A-3D also sets new standards in its ability to maintain several internal operating points, allowing it to hop quickly and seamlessly between frequencies.

¹⁴e.g. EN61000-4-6 Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields: Level 3.

¹⁵i.e. its -3dB frequency response.

¹⁶Invented c. 1942 for guided torpedo anti-jamming.

¹⁷the sampling window imposes a $\frac{\sin(x)}{x}$ frequency response characteristic which is full of slowly reducing lobes and few, very narrow gaps to hop to.

To further protect the AX112A-3D against EMI, the signal path in the analogue front end, uses techniques to avoid its amplifiers from over-ranging in the presence of very high levels of interference. Even when such countermeasures are employed, the touch report stability is still industry leading, thanks to the high SNR of the acquisition engine.

So far we have talked only about immunity to interference, but in some applications, emissions are just as big an issue. The AX112A-3D drives the sensor with a pure 1.25V amplitude sinusoidal waveform at a single frequency. Compare this to many competing devices that drive the sensor using a square wave at up to 30V peak-to-peak, leading to problems when trying to pass emissions certification.

6.8 Water Suppression

The AX112A-3D employs a unique architecture that allows it to make two types of measurement during the same frame: i) trans-cap (as already discussed) and ii) a second measurement type called *absolute capacitance* or *abs-cap*. Abs-cap measures the total capacitance of an electrode, rather than the coupling capacitance to another electrode. When abs-cap measurements are taken, they are done concurrently on a whole group of electrodes. This means that multiple electrodes are driven with near identical waveforms and hence the coupling capacitance from neighbour to neighbour is virtually neutralized; only the total capacitance of each electrode to GND+earth is sensed. This has the useful side-effect that water puddles, laying on the CTS lens surface that bridge between/across electrodes, become almost invisible from a capacitance point of view. Trans-cap measurements, on the other hand, will see normal touches and water puddles as almost identical. By making two types of measurement, the AX112A-3D can discriminate between such contacts and hence can offer a great improvement in *waterproofing* the overall touch solution.¹⁸

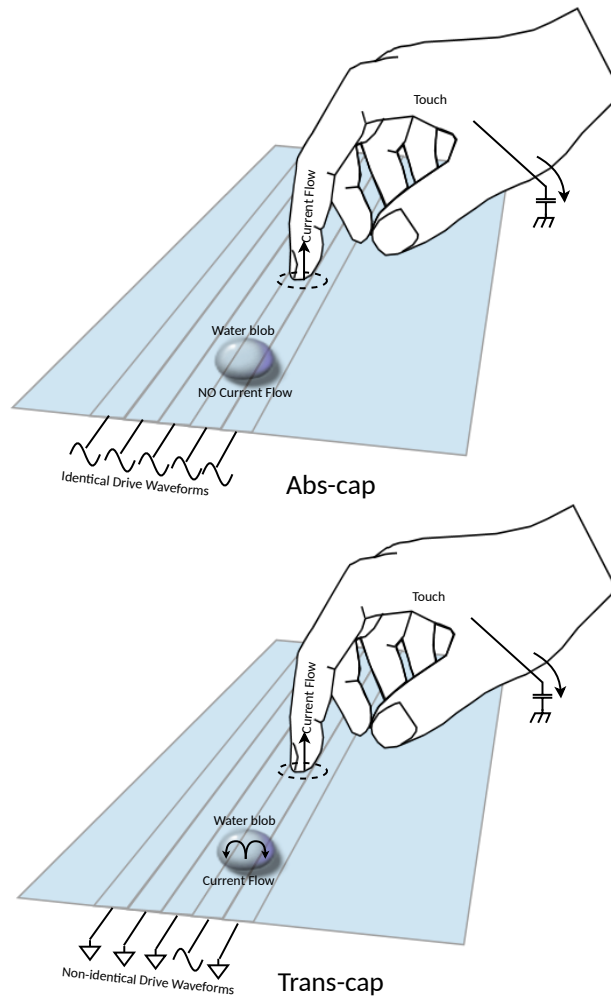


Figure 6.8-1: Different Behaviors With Abs-cap and Trans-cap Measurements With Water and Touch

¹⁸These effects have been well known since the late 90's but implementation of dual measurement-mode controllers only became popular with the growth of mobile devices.

Abs-cap measurements come with their own set of challenges, mainly caused by the fact that the change in capacitance with touch, is a much smaller proportion of the electrode's *baseline capacitance* than it is with trans-cap¹⁹. This leads to a requirement for even greater measurement SNR. There are ways to mitigate some of the extra capacitive loading on the electrodes, particularly those that live at the edges of the CTS, that would normally be exposed large areas of GNDed conductor (e.g. other traces, ESD rings etc). See **Appendix B References** for links to application notes that cover this topic in more detail.

During a frame, the AX112A-3D typically measures a 2DCTS in trans-cap mode across many sub-frame time slots (See **6.1 Sensing Overview**). Additionally, it will use multiple slots to measure the CTS in abs-cap mode. TouchHub2 software can create a configuration file that will schedule all of these measurements automatically.

¹⁹i.e. the touch delta percent is smaller because the baseline capacitance is so much higher (perhaps 10 to 100 times that of a trans-cap node).

6.9 Sensor Compatibility

The wide measurement range of aXiom devices means they can operate with most sensor styles and constructions. For further details refer to **TNxAN00042 aXiom Touch Controller Sensor Compatibility**.

6.10 Sensor Protection

Touch sensors are fabricated using a range of materials, some of which are extremely stable and some of which are not. Indium Tin Oxide (ITO), for example, commonly used to make the sensor's electrodes, is a ceramic conductor²⁰ that is remarkably robust to environmental damage caused by high temperature and humidity. It is very common to leave ITO exposed to the environment, even in harsh conditions²¹. Other materials, notably the Silver commonly used to form the edge wiring on sensors, is a very different proposition when exposed to such conditions and when it is also supporting a voltage difference to a neighbouring conductor. In these conditions, an effect known as Electro-Migration can occur over time, that forms small conductive "dendrites" between traces that eventually short-circuit the touch sensor channels and cause premature failure. This is true for sensors that are fabricated on glass or plastic substrates. A common requirement in industrial and automotive environments, is to achieve a 504 hour operating life when exposed to 60°C and 90% relative humidity. This requirement sounds easy enough and indeed, many claim that their sensor/controller combination can pass this test. The reality is that the test is often conducted like a "storage" test with no power applied during the environmental exposure. This is *not* the same test! It is the application of power, and hence voltage, that causes the Electro-Migration. The rate of migration depends on many factors including the voltage differential between traces.

For this reason, the AX112A-3D takes two special precautions:

1. It uses a very small drive amplitude of 1.25V (2.5V pk-pk) to measure the capacitance. Compare this to controllers that use 10V to 30V to drive the sensor.
2. It also biases all inactive electrodes in such a way that, all active drive voltages swing symmetrically either side of this bias; this has the effect of further slowing migration as the net DC level is approximately zero²². Compare this to controllers that bias inactive electrodes to GND and drive with a pulsed 30V waveform.

Further discussion of these effects are beyond the scope of this document, but further information can be found in **Appendix B References**.

²⁰It can also be classed as an alloy depending on its exact composition.

²¹Noting that standing water or other contaminants can etch ITO if they are acidic in nature.

²²Referred to as a DC neutral drive.

7 Host Interfaces

7.1 Available Interfaces

The AX112A-3D offers two ways to communicate with the host:

1. A slave I²C interface, consisting of the following pins (taking the name **before** the “/”): (**SLVSDA / SCK**), (**SLVSCL / nSS**) and an interrupt (**SLVnIRQ**). Rates up to 400KHz are supported.
2. A slave SPI interface, consisting of the following pins (taking the name **after** the “/”): (**SLVI2CADDRSEL / MOSI**), (**nSLVI2C / MISO**), (**SLVSDA / SCK**), (**SLVSCL / nSS**) and an interrupt (**SLVnIRQ**). Rates up to 4MHz are supported.

7.2 Mode Selection

A single pin controls which host interface is selected: **nSLVI2C / MISO**. The pin is sampled as the device starts up (from a power on, or reset event):

If the pin is sampled low, **Slave I²C** mode is selected.

If the pin is sampled high, **Slave SPI** mode is selected.

The pin includes a weak pull-up that must be overridden either by tying it to GND, (for I²C mode) or by **pulling up** with a supplemental resistor to VDDI (for SPI mode)²³ (see **4.9 nSLVI2C / MISO**).

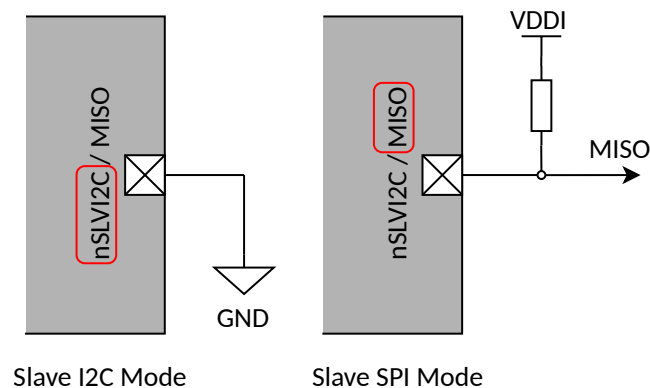


Figure 7.2-1: Communication Mode Selection

²³In SPI mode the pin changes to become an output and hence must **not** be pulled up by tying directly to VDDI.

7.3 Slave I²C Mode

7.3.1 Slave Address Selection

Two different Slave I²C addresses can be selected with the **SLVI2CADDRSEL / MOSI** pin. The pin is sampled as the device starts up (from a power-on, or reset event):

SLVI2CADDRSEL / MOSI level	Slave I ² C Address (7-bit hex)
low	0x66
high	0x67

Table 7.3.1-1: Slave I²C Address Selection

See 4.8 **SLVI2CADDRSEL / MOSI** for notes on terminating this pin.

7.3.2 Connections

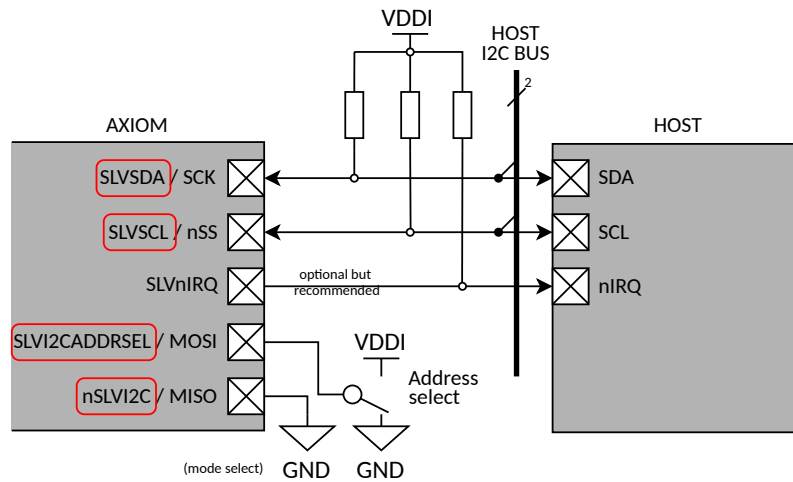


Figure 7.3.2-1: Slave I²C Connections

7.3.3 I²C Protocol

The communications protocol used to access configuration registers in the device and to receive event reports from the device, can be found in **TNxAN00035 aXiom Touch Controller Comms Protocol**. Real-time report collection from the device over the I²C interface, has been optimized to work in an interrupt driven mode rather than being polled.

7.4 Slave SPI Mode

7.4.1 Device Selection

In order to communicate with the device, the **SLVSCL / nSS** pin must be asserted low for (at least) the duration of the communication. It is OK to permanently connect **SLVSCL / nSS** to GND when in SPI mode, if the AX112A-3D is the only device on the SPI bus.

7.4.2 Connections

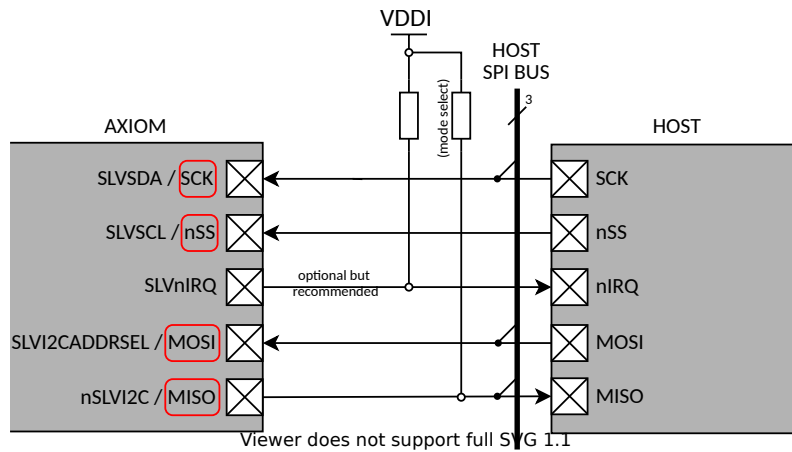


Figure 7.4.2-1: Slave SPI Connections

7.4.3 SPI Protocol

The SPI interface operates in Mode 0²⁴. The communications protocol used to access configuration registers in the device and to receive event reports from the device, can be found in **TNxAN00035 aXiom Touch Controller Comms Protocol**. Real-time report collection from the device over the SPI interface has been optimized to work in an interrupt driven mode rather than being polled.

²⁴Clock Polarity:0, Clock Phase:0, Clock Edge:1 (Clock idles at 0, and uses rising edge to sample data, and uses falling edge to shift data).

8 Haptics

In order to provide physical sensation feedback to a user who is touching and-or pressing on a surface, the AX112A-3D offers a mechanism to trigger a 3rd party Haptic driver device. To qualify when a Haptic effect should be played, the following events can be used to generate the overall trigger:

- Touch position.
- Touch movement.
- Applied force (rising).
- Applied force (falling).

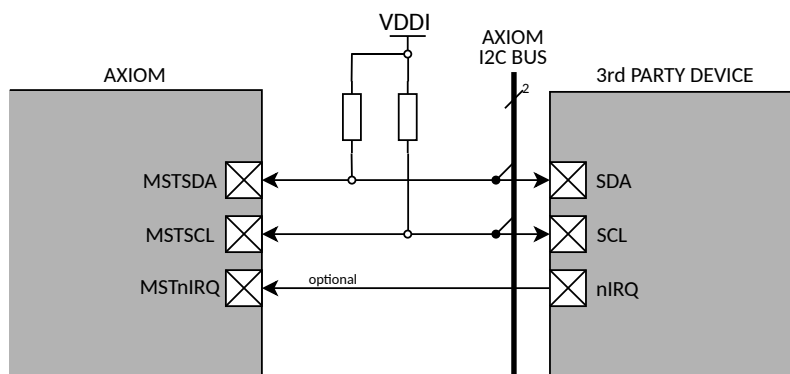


Figure 8-1: Master I²C Connections to 3rd Party Device(s)

The qualification by touch position is controlled using an array of configurable hot-spots over the 2D surface. Each hot-spot can be switched on and off efficiently, allowing the host to change UI screens (and selected hot-spots) smoothly. Hot-spot definition is sufficiently fine-grained to allow rectangular closed-form regions to be defined. Each hot-spot can be triggered based on a number of criteria and can also trigger a specific effect using the Master Comms interface. Additionally, hot-spots can be tagged in groups to allow their XY positions to be globally offset, allowing grouped hot-spots to be *scrolled* in synchronism with a UI.

aXiom can use the Master Comms port in one of 3 modes to trigger the playback of an effect:

1. In Master GPIO mode; driving a set of 4 output pins to control an actuator. (normally via a power amplifier such as a motor driver).
2. In Master I²C mode²⁵; using the Master I²C interface to send commands to trigger a 3rd party actuator device.
3. In Master SPI mode²⁶; using the Master SPI interface to send commands to trigger a 3rd party actuator device.

The first method is limited in that it only allows simple effects to be triggered. The second and third methods are much more flexible, as they can transmit a sequence of commands to a device that both define and trigger the effect. A typical example of such a 3rd party actuator device is the Texas Instruments™ DRV2605. This can be connected to the Master Comms port I²C interface of the AX112A-3D and a series of I²C *macro* commands can be defined in the device configuration, to achieve various effects. As part of the I²C sequence, dynamic data can be sent to the device from the AX112A-3D such as X, Y, touch number, force value, effect etc.

For further details see **TNxAN00036 aXiom Touch Controller Haptics Drive**.

²⁵Noting that this is not related in any way to the **Host** Interface I²C Mode.

²⁶Noting that this is not related in any way to the **Host** Interface SPI Mode.

9 Programming Model

aXiom devices use a register interface called *Touch Controller Protocol*, or TCP, which defines each and every register in the device, how they are organized and accessed. TCP covers configuration and tuning registers, as well as general status and information registers. For the transport of “live” data, TCP also describes a reporting scheme; this is particularly important for host device drivers, because it is the mechanism by which the device sends real-time touch information to the host.

While all aXiom devices use TCP, the exact set of registers and features offered by a specific device do vary. Hence, this general document does not present a detailed programming interface. Instead, you are directed to **TNxAN00038 aXiom AX112A Touch Controller Programmer’s Guide**.

The runtime firmware in aXiom devices is field upgradable using a command and register interface called “Bootloader Protocol” or BLP, details of which can be found in **TNxAN00043 aXiom Touch Controller Bootloader**.

10 Device Characteristics

All quoted ranges are at an operating ambient temperature of 25°C unless otherwise stated.

10.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 10.1-1 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these, or any other conditions beyond those indicated in 10.2 Operational Ratings is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Units
VDDA	Analogue supply	-0.3	4	V
VDDI	I/O supply	-0.3	4	V
V _{pc}	Voltage applied to any CMOS pin	-0.5	VDDI+0.5	V
I _{pc}	Maximum source/sink current for any CMOS pin	-25	25	mA
V _{pa}	Voltage applied to any Analogue pin	-0.5	VDDA+0.5	V
I _{pa}	Maximum source/sink current for any Analogue pin	-25	25	mA
T _s	Storage temperature (non operating)	-65	150	°C
T _J	Junction temperature (operating)		125	°C
ESD _{hbm}	ESD rating, human body model ²⁷		2000	V
ESD _{cdm}	ESD rating, charged device model ²⁷		750	V

Table 10.1-1: Absolute Maximum Ratings

²⁷Discharge direct to device pins. Discharge rating to the sensor/lens in a system is application specific but is typically far higher than this device rating.

10.2 Operational Ratings

10.2.1 Operating Conditions

Symbol	Parameter	Range	Units
T _A	Ambient temperature ²⁸	-40 to +105	°C
RH _A	Ambient relative humidity (non-condensing)	10 to 90	%RH

Table 10.2.1-1: Operating Conditions

10.2.2 Power Requirements

Symbol	Parameter	Range²⁹	Units
VDDA	Analogue supply	2.97 to 3.63	V
VDDI	I/O supply	1.62 to 3.63	V
IDDA	Active analogue supply current (average over frame)	200 to 250	mA
IDDI	I/O supply current (average over frame)	0.005 to 5	mA
N _{VDDA}	Allowable peak-to-peak noise and ripple on analogue supply	85	mV
N _{VDDI}	Allowable peak-to-peak noise and ripple on I/O supply	200	mV

Table 10.2.2-1: Power Requirements

Note that IDDA varies depending on the device’s configuration, which defines the measurement types and durations that are performed. For host power supply sizing and thermal calculations, the maximum stated value should be used as an average, with an allowance for +/-25% current variation away from the average during a measurement frame. The chosen regulator must be able to cope with this transient current behaviour. Generally, a device configuration that employs only Trans Cap measurements, will consume considerably less than one which also enables Abs Cap measurements, that last for a significant percentage of the total frame time.

Also note that IDDI varies significantly depending on the amount of IO activity, but is generally far smaller than IDDA. As noted in **4 Pin Descriptions** VDDA and VDDI are commonly shared and so this current should be added to the overall supply current budget.

10.2.3 Power Sequencing

There are no power sequencing requirements for the application or removal of (or between) VDDA and VDDI. Internal brown-out detection will prevent the device from operating, until both VDDA and VDDC (internal) are properly established. VDDI is not level checked as it does not directly impact the internal operation of the device³⁰.

CMOS I/O pins should never exceed the limitations stated in Table **10.1-1** (Vpc and Vpa) during power up, operation or power down.

During power-up, while the power rails are stabilising, the voltage levels on the I/O pins may be undefined and should not be relied upon for deterministic behaviour.

10.2.4 Startup Time

From the rising edge of **nRESET** (or when **VDDA** rises above approx. 2V) to the falling edge of **nIRQ**³¹: < **110ms** typical. At this point the device is fully operational.

²⁸Subject to appropriate PCB design.

²⁹Treat these values as bounding limits

³⁰...but clearly VDDI needs to be correctly established in order to communicate with the device.

³¹The first interrupt is created by a “hello” System Manager report to the host.

10.2.5 Reduced Power Mode

To conserve power during periods of low activity, the device can be configured to enter³² a Reduced Power Mode (RPM). This trades off first detection latency (from RPM) against power consumption. Typical power reductions of 2 to 6x are possible, as the RPM measurement rate is reduced. For further details refer to **TNxAN00061 aXiom Touch Controller Reduced Power Mode**.

³²Either automatically or by command.

10.2.6 CMOS I/O Characteristics

Symbol	Parameter	Range	Units
V_{IL}	Logic low input @ 1.8V VDDI	-0.3 to 0.63	V
V_{IH}	Logic high input @ 1.8V VDDI	1.2 to 3.6	V
V_{OL}	Logic low output @ 1.8V VDDI, 1.5mA sink	0.5 max	V
V_{OH}	Logic high output @ 1.8V VDDI, 1.5mA source	1.4 min	V
R_{WPU}	Weak pull up resistance @ 1.8V VDDI (where applicable)	69 - 201	K Ω
I_{IL}	Input leakage current	± 1 max	μ A

Table 10.2.6-1: CMOS I/O Characteristics (1.8V)

Symbol	Parameter	Range	Units
V_{IL}	Logic low input @ 3.3V VDDI	-0.3 to 0.8	V
V_{IH}	Logic high input @ 3.3V VDDI	2.0 to 3.6	V
V_{OL}	Logic low output @ 3.3V VDDI, 4mA sink	0.5 max	V
V_{OH}	Logic high output @ 3.3V VDDI, 4mA source	2.4 min	V
R_{WPU}	Weak pull up resistance @ 3.3V VDDI (where applicable)	34 - 74	K Ω
I_{IL}	Input leakage current	± 1 max	μ A

Table 10.2.6-2: CMOS I/O Characteristics (3.3V)

10.2.7 Slave I²C Characteristics

The AX112A-3D implements a Slave I²C interface that is compliant with industry standards. It supports both Standard-mode (100KHz) and Fast-mode (400KHz). Addressing is 7-bit. Clock stretching support by the host is required.

Bus timings are as per **UM10204 I²C-bus specification and user manual Rev. 6 — 4 April 2014**. The general form of an I²C transaction is shown below. Additional I/O and timing parameters can be found in the aforementioned document in Table 9 and Table 10.

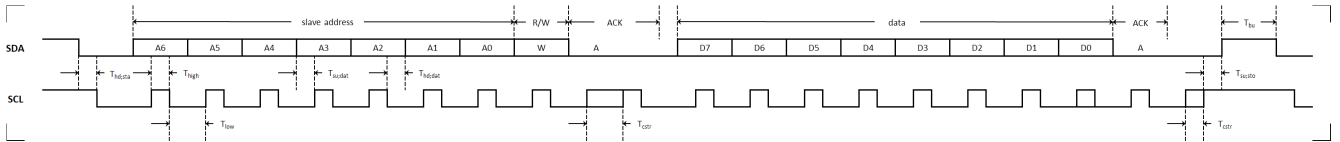


Figure 10.2.7-1: Typical I²C Transaction and Parameters

Symbol	Parameter	Min	Max	Units
T _{hd;sta}	Start bit hold time	600	-	ns
T _{high}	Clock high period	600	-	ns
T _{low}	Clock low period	1300	-	ns
T _{su;dat}	Data setup time	250	-	ns
T _{hd;dat}	Data hold time	0	-	ns
T _{cstr}	Maximum clock stretch by slave	-	5	us
T _{su;sto}	Stop bit setup time	600	-	ns
T _{bu}	Bus free time between stop and start	1300	-	ns

Table 10.2.7-1: Timings

10.2.8 Slave SPI Characteristics

The AX112A-3D implements a Slave SPI interface that is compliant with industry standards. It supports Mode 0 communication at up to 4MHz. The most significant bits of 8-bit data fields are exchanged first.

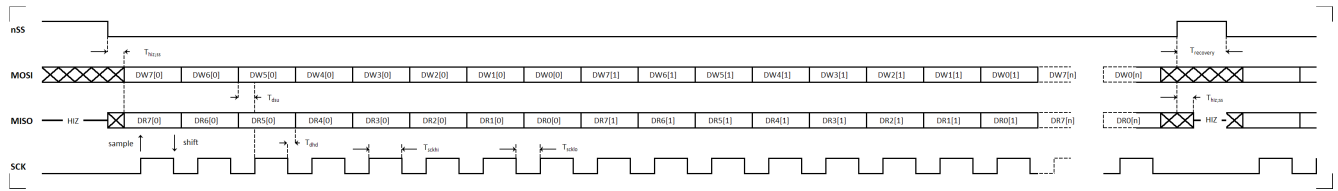


Figure 10.2.8-1: Typical SPI Transaction and Parameters

Symbol	Parameter	Min	Max	Units
$T_{hiz:ss}$	nSS transition to MISO transition to/from HiZ	-	20	ns
T_{dsu}	Data setup time (MOSI to SCK)	20	-	ns
T_{dhd}	Data hold time (SCK to MISO)	50	-	ns
T_{sckhi}	SCK high period ³³	100	-	ns
T_{scklo}	SCK low period ³⁴	100	-	ns
$T_{recovery}$	Slave recovery time, ready for next transfer ³⁵	-	45	us

Table 10.2.8-1: Timings

³³Subject to maximum SCK frequency of 4MHz.

³⁴Subject to maximum SCK frequency of 4MHz.

³⁵The host must ensure that it does not violate this recovery time by ensuring that transfers are spaced apart sufficiently to let the slave prepare for the next transfer. Violating this timing will result in undefined Slave behaviour, possibly lasting beyond the initial violated transfer.

10.2.9 Master I²C Characteristics

The Master I²C interface implemented in the AX112A-3D is intended for communication with one or more 3rd party slave devices. The characteristics of the interface are identical to those of the Slave I²C interface. See **10.2.7 Slave I²C Characteristics** for details. The Master I²C interface supports clock stretching by a connected slave.

10.2.10 Capacitance Ranges and Drive Limits

Symbol	Parameter	Absolute min	Recommended min	Recommended max	Absolute max	Units
F_{EXC}	Excitation frequency	50	100	500	1000	KHz
$V_{EXC-TRANS}$	Trans Cap excitation voltage pk-to-pk (centered around $VDDA/2$)	0	2.5	2.5	$VDDA-0.6$	V
$V_{EXC-ABS}$	Abs cap excitation voltage pk-to-pk (centered around $VDDA/2$)	0	2.4	2.4	$VDDA-0.9$	V
$C_{SHIELD2DCTS}$	Total capacitance to GND on SHIELD2DCTS	-	-	-	20	nF
$C_{SHIELDAUX}$	Total capacitance to GND on SHIELDAUX	-	-	-	20	nF
$C_{ABCD-TRANS}$	Total Trans Capacitance load on only A, B, C or D pin	0.5	1.25	2.5	5	pF
$C_{ABCD-ABS}$	Total Abs Capacitance to GND on only A, B, C or D pin	20	-	200	500	pF
$C_{AUX-ABS}$	Total Abs Capacitance to GND on only AUX pin	20	-	-	1000	pF

Table 10.2.10-1: Capacitance Ranges and Drive Limits

Note that F_{EXC} , $V_{EXC-TRANS}$, $V_{EXC-ABS}$ can be directly controlled via the device’s configuration registers, so ensuring that the limits are met by tuning. The capacitance limits relate to external factors arising from the attached sensor and associated tracking.

Symbol	Parameter	Value	Tolerance	Dielectric	Units
C_{REFCAP}	REFCAP reference capacitor	220	1%	NP0 / C0G	pF

Table 10.2.10-2: REFCAP Requirements

10.2.11 Non-volatile Memory Characteristics

Symbol	Parameter	Range	Units
N_{EC}	Number of erase cycles	10000	cycles
t_{DR}	Data retention @ 85°C T _A	10	years
EDAC	Error detection and correction	Detect and correct all 1-bit errors Detect all 2-bit errors	-

Table 10.2.11-1: Non-volatile Memory Characteristics

10.2.12 Device BIST Capabilities

- RAM self tests.
- NVM EDAC (see **10.2.11 Non-volatile Memory Characteristics**).
- Code execution protection using Watchdog Timer clocked by separate internal oscillator.
- Checksum over NVM.
- Checksum over volatile configuration.
- Checksum over non-volatile configuration.
- Out of range VDDA detection.
- Out of range Acquisition Engine reference capacitor checks.
- Interrupt pin test.
- Cross-check main CPU and RTC/watchdog oscillators against each other.
- Configurable "Heartbeat" report to host allows BIST trigger (limited range) and live status plus, a cross check of the timing period/CPU main oscillator rate.

10.2.13 Sensor BIST Capabilities

- All sense channels allow detection of CTS and CDS impedance leakage of up to 200K Ω to any net.
 - Test can be triggered by host command and optionally run at device boot-up.
- Detection of opens on CTS and CDS electrode channel by configurable signal limits.
 - Test can be triggered by host command and also run periodically using Heartbeat tick.
- Separate signal limit tests for Trans Cap, Abs Cap and AUX.
- Separate test limits for the middle, edges and corners of a CTS (Trans Cap mode) to improve fault coverage.

10.2.14 2D CTS Diagonal Size Range Guide

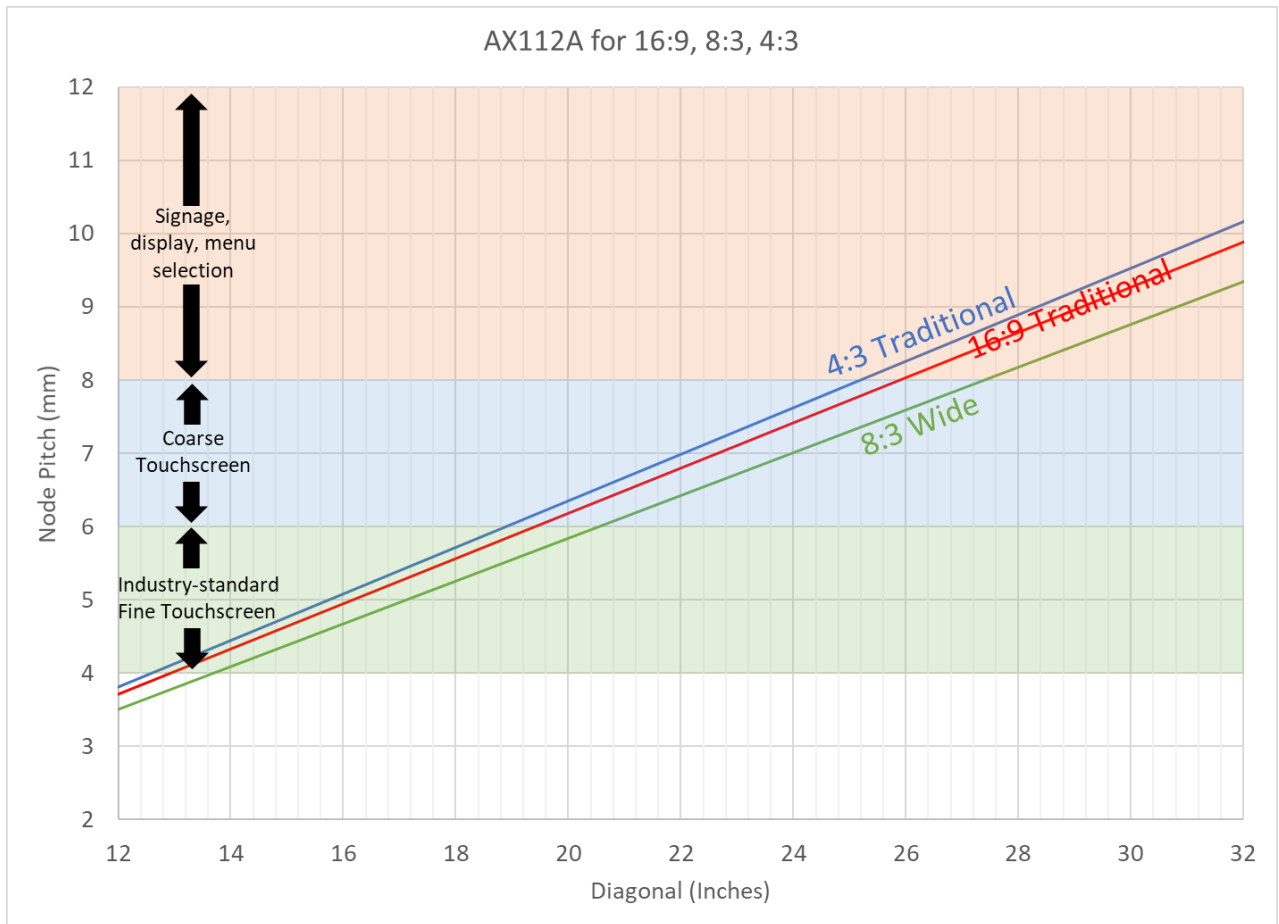


Figure 10.2.14-1: 2D CTS Diagonal Size Range Guide

Appendix A Package Drawings

A.1 LQFP156-EP14201404

A.1.1 Package Information

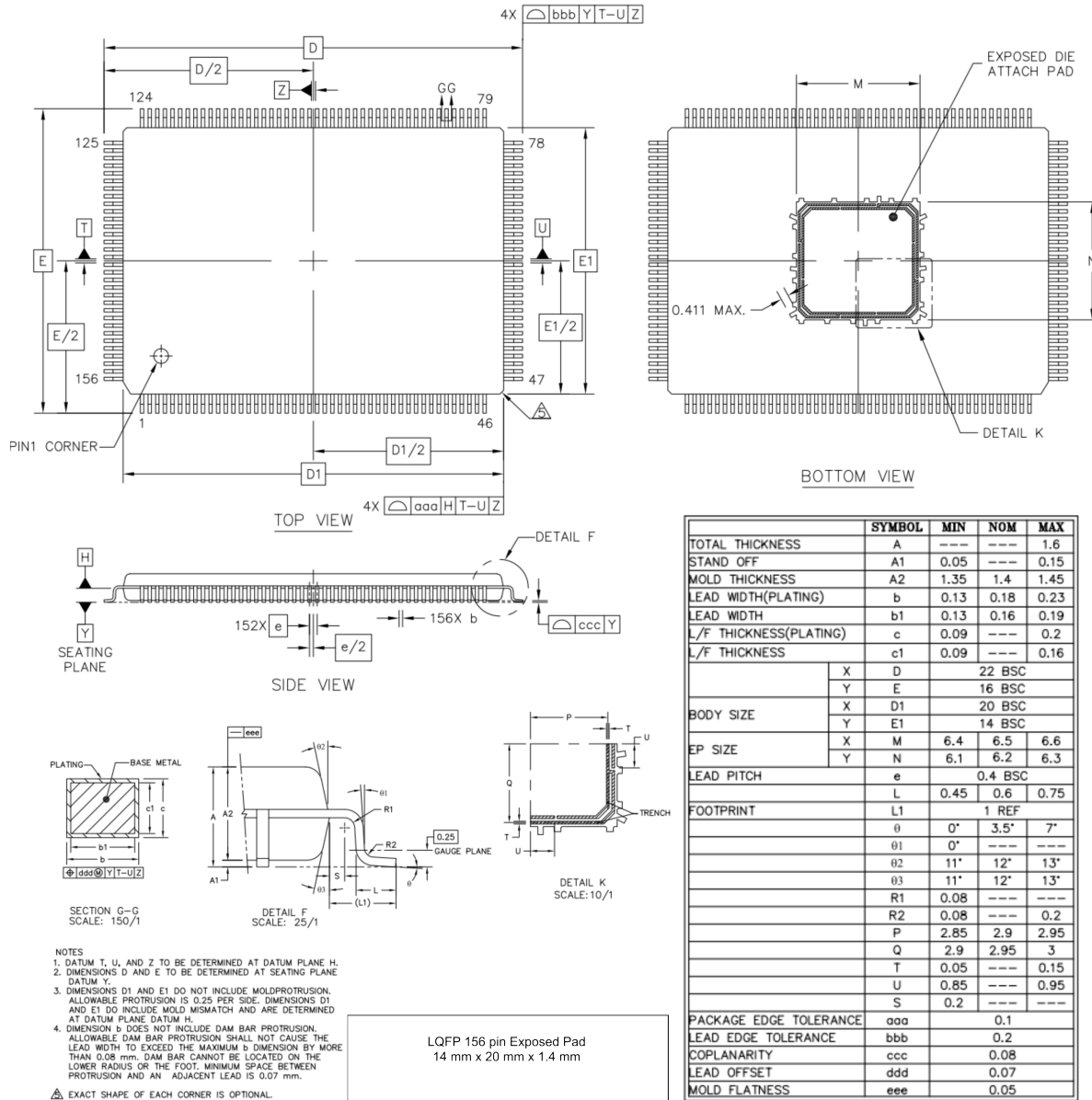


Figure A.1.1-1: Package Drawing

A.1.3 Layout and Routing Considerations for VDDA tracks

To maximize SNR performance, special care must be taken when laying out VDDA power traces.

The maximum tolerated voltage drop *between* VDDA pins varies. The table(s) below should be used for estimation of device current consumption into each pin to allow calculation of the (I*R) voltage drops in your PCB layout. You must then check that they are within the allowed range as listed below.

Pin	Type	Max Current (mA)	ΔV
23	VDDA	30	<2mV ΔV between these pins
47	VDDA	50	
156	VDDA	50	
85	VDDA	5	<5mV ΔV from other VDDA power pins
111	VDDA	200	<5mV ΔV from other VDDA power pins
118	VDDA	5	<5mV ΔV from other VDDA power pins

The images provided are for general guidance. Gerber files for reference designs can be provided by TouchNetix on demand.

Please note: any reference material provided shall be taken as guidance only. PCB designers must ensure to run power/current analysis on their designs to make sure they are compliant with the requirements outlined above.

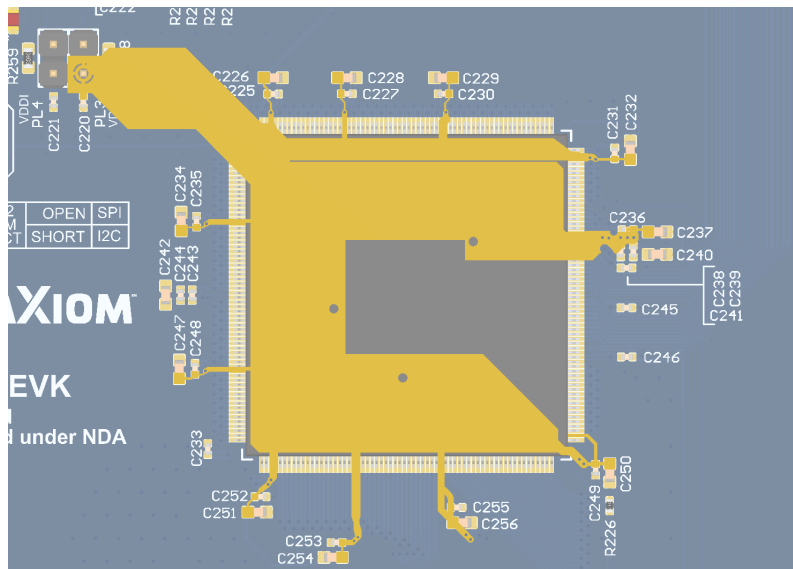


Figure A.1.3-1: C-shaped power routing, balanced amongst all VDDA pins. Figure shows an AX198A, same advice can be applied to this device.

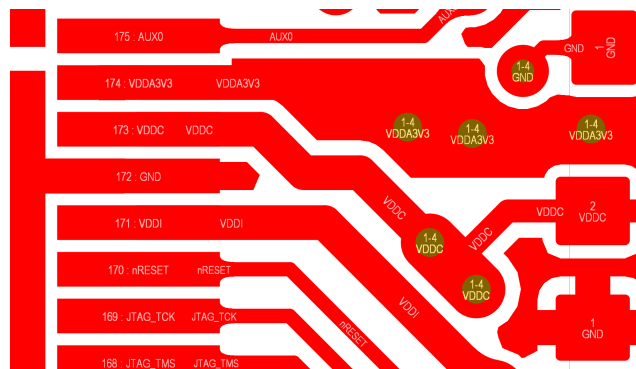


Figure A.1.3-2: Note the use of the widest possible tracking and multiple vias for all VDD tracks. Figure shows an AX198A, same advice can be applied to this device.

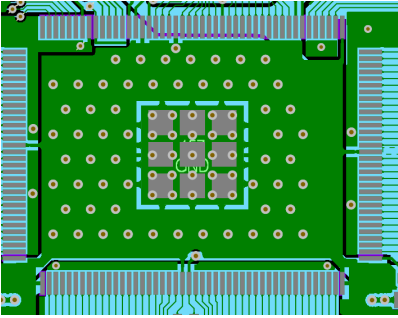
A.1.4 Package Thermal Characteristics

θ_{JA} (junction to ambient ³⁶) : 21.5oC/W.

A.1.5 PCB Footprint Notes

The LQFP156 package has an exposed centre GND pad that must be soldered and via'd to suitable copper regions on a 4-layer PCB to help improve the thermal conductivity from junction to ambient. Follow these rules to achieve the stated thermal performance:

1. Use a centre GND PCB pad (to connect to device's exposed pad) which is 6mm x 6mm, using a solder paste stencil that is cross hatched (e.g. 1.5mm square pads) to avoid excessive solder.



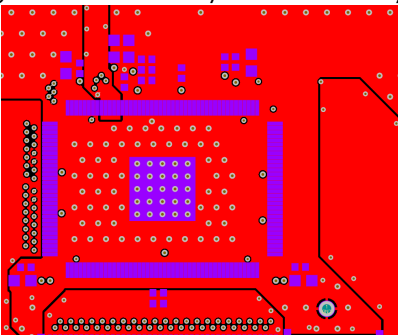
2. The centre pad must have a minimum of 25 off, 0.3mm diameter, plugged³⁷ vias connecting to GND floods on the layers below.

3. Signal traces should not be routed under the device body, to allow maximal copper flood under the device body, without adding capacitive burden to the driven shield signals³⁸.

4. Where possible, use 2oz copper (finished) on the PCB outer layers to improve heat flow.

5. Use a GND flood that extends on each layer up to the device pins, under the entire device body area (noting that power trace(s) will likely need to bisect the flood on one inner layer).

6. Use extra 0.3mm regular or plugged vias placed on a 1.5mm pitch to "stitch" the GND floods together electrically and thermally under the device.



7. Extend a copper GND flood from underneath the body, past the non-sensing pins (i.e. predominantly on one package edge) on the bottom layer of the PCB, to create an extra area of at least 25mm x 25mm. Keep this area wide and continuous and avoid adding narrow necks or meanders, so that the area functions as a good thermal conductor away from the device.

8. If uncertain, please contact TNx.

The above rules assume a 4-layer (minimum) PCB and that the design goal is to meet 105°C ambient temperature operation. In situations where a lower operating temperature is required (e.g. Industrial/Medical), these rules can be relaxed to a 2-layer PCB, but special care should be taken to optimize the outer layer copper floods on the rear side, to allow enough heat to flow away from the device.

³⁶When soldered to PCB as described in **A.1.5 PCB Footprint Notes**.

³⁷To avoid solder wicking from under the body during reflow.

³⁸maximum added capacitance to the SHIELD2DCTS or SHIELDAUX nets must not be greater than 100pF.

Appendix B References

TNxAN00035 aXiom Touch Controller Comms Protocol.
TNxAN00037 aXiom Touch Controller Sensor Channel Routing.
TNxAN00043 aXiom Touch Controller Bootloader.
TNxAN00045 aXiom Touch Controller Comms Quick Start Guide.
TNxAN00048 aXiom Touch Controller EMC Report.
TNxAN00051 aXiom Driver Guide.
TNxAN00052 aXiom Project Flow.
TNxAN00056 aXiom Self Test.
TNxAN00061 aXiom Touch Controller Reduced Power Mode.
TNxD00442 Production Process with aXiom Devices.
TNxAN00036 aXiom Touch Controller Haptics Drive.
TNxAN00041 aXiom Touch Controller 3D Prox and Hover.
TNxAN00053 aXiom Touch Controller 3D Gestures.
TNxAN00062 aXiom 3D HID Digitizer Support.
TNxAN00079 aXiom Dial on Display.
TNxAN00047 aXiom Touch Controller Sensor Testing.
TNxAN00042 aXiom Touch Controller Sensor Compatibility.
TNxAN00046 aXiom Touch Controller Multi Press Demo Guide.
TNxAN00085 aXiom Force Sensing.
TNxAN00038 aXiom AX112A Touch Controller Programmer's Guide.
TNxAN00044 aXiom Touch Controller AX112A EVK Quick Start Guide.

Note: Release of the above documents may require a specific NDA to be in place, please contact TouchNetix for more details.

Appendix C Legal Copyright and Disclaimer

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Appendix D Document History

Revision	Date	Change summary
A1	02/07/2019	Preliminary release.
A2	27/08/2019	Add further comments regarding VDDI domain IO pins relative to VDDI state.
A3	28/09/2019	Add reference schematic for LQFP176. Clarify VDDA pin (LQFP176:pin 22 LQFP156:pin 23).
A4	15/11/2019	Change pin-out for LQFP156, update LQFP156 EP package drawing & ordering codes.
A5	23/12/2019	Replace LQFP176 reference schematic with LQFP156.
A6	04/02/2020	Add details for region/button support.
A7	05/05/2020	Add details for SPI master comms support for Haptics. Correct bypass cap recommendations on VDD rails.
A8	01/06/2020	Remove LQFP176 references. Add PCB footprint layout notes for LQFP156.
A9	04/06/2020	Add 2D CTS diagonal size guide.
A10	25/06/2020	Add capacitance range data and adjust IDDA notes. Update BIST information.
A11	23/07/2020	Change connection advice for unused sense pins.
A12	10/08/2020	Correct SLVnIRQ pin type. Add timing data for I2C and SPI.
A13	03/09/2020	Add section about Dial On Display.
A14	10/11/2020	Improve slave interface diagrams.
A15	21/01/2021	Update ref. schematic and notes to add 1nF to SHIELD2DCTS. Update screen diagonals plot.
A16	15/02/2021	Add notes about Reduced Power Mode, shipping tray details.
A17	06/04/2021	Add tuning header in ref schematic.
A18	21/06/2021	Add sensing architecture diagram.
A19	22/07/2021	Improve package drawing.
A20	19/11/2021	Add power requirements detail. Formatting clean ups.
A21	28/02/2022	Updated ordering information..
A22	28/03/2022	Added VDDA layout considerations.

Revision	Date	Change summary
B1	12/06/2022	Rename to 3D variant. Include AUXn reference caps.
B2	19/08/2022	Add more details for reference caps.
B3	23/10/2022	Updated grammar and punctuation, updated pin table to superscript I ² C entries.
B4	23/03/2023	Correction to the Absolute Maximum Ratings table for Ts and Tj values, split IO tables into 1.8V and 3.3V levels and change measurement criteria for VOH from max to min.
B5	24/03/2023	Addition of B Pin restrictions to the Pin Description table
B6	07/09/2023	Update of a disclaimer to the reference page to highlight that before access is permitted to some documents, an NDA is required. Some referenced documents are hidden from the reference list as not currently shared in the document pack, no longer a used document or not released. Updated reference link for new Dials on display document and added to the reference list. Update Dial on Display description. Update the details in the Force Sensing section that describes how the reference capacitors are to be connected. Update reference schematic to demonstrate how the reference capacitors should be placed.
B7	28/03/2024	nReset capacitor value corrected to 10nF from 20nF. Added labels to the reference capacitors on the reference schematic plus brief explanation regarding AUX channel.
B8	01/10/2024	Changes made to the reference schematics.
B9	11/10/2024	Added Footprint information and Bootloader part number details. Removed redundant documentation and updated Reference table.
B10	03/02/2025	Correct reference cap text in AUX0..3 description. Remove regions. Added information to the power sequencing section regarding the state of the I/O pins at power-up.